QBLOX

QCM / 0-400 MHz
Qubit Control Module | Cluster Series 19" Rack Mounted

Description

A Qubit Control Module (QCM) hosts 6 sequence processors for flexible multi-plexed driving and tracking of up to 6 qubits (or other oscillators). The unleveled noise performance makes it ideal for high-fidelity single- and two-qubit control.

The extremely low offset and gain drift (a few ppm/K) avoid the need for frequent recalibration. This makes the QCM the ideal baseband signal generator to push gate fidelities to the next level.

Advanced sequencer capabilities drastically speed up characterization experiments (Spectroscopy, Rabi, Chevron, Charge-stability diagrams) by avoiding repeated wave uploading and large overhead in software-controlled loops.

During quantum algorithms, it allows for instance arbitrary single-qubit control (phase, amplitude) from a single pulse pair. Qubit phases can be tracked in real time using the NCOs which accept virtual Z-gates through phase updates from the sequence processor.

FASTEST RISETIME FOR RING-FREE PULSES
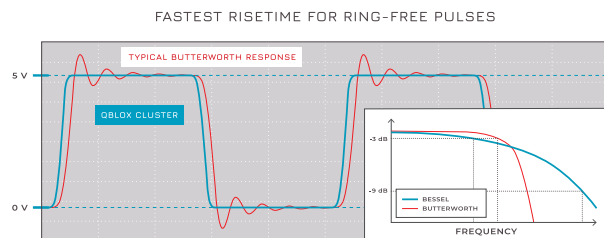
Cluster modules are equipped with Bessel type filters to generate ring-free pulses with fast rise time as required by quantum computing applications.

The commonly used Butterworth type filters (higher -3dB point) need further filtering to overcome the overshoot and ringing effects, which in turn results in longer rise times. Bessel type filters provide the sharpest step responses with a larger bandwidth beyond -3 dB point as illustrated in the figure.

Features

- Advanced distributed sequence processing.
- Multiplexed control of up to 6 frequencies.

- Base-band operation (4 independent channels) or IQ-mode (2 channel pairs) for single-sideband upconversion.

- Offset instructions allow constructing arbitrarily long (modulated) signals.

- Synchronized to all other modules with SYNQ protocol.
- Real-time modulation and mixer corrections.

- External instrument control by 4 marker outputs.

- Real-time control: amplitude, offset, modulation frequency, modulation phase (virtual Z-gates).
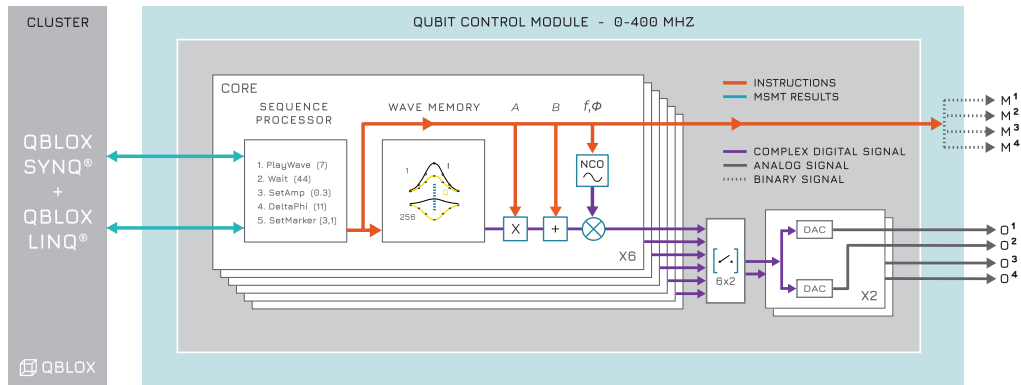
Specifications

Analog output channels	4	Gain stability, 500 mVpp into 50 Ω, 15-32 °C ambient	2.3 µV/K = 4.6 ppm/K
DAC sample rate	1 GSPS	Offset stability, into 50 Ω, 15-32 °C ambient	5 µV/K = 1 ppm w.r.t full scale
DAC resolution	16 bit	Binary output markers	4 (3.3V LVTTL)
Trigger Latency	110 ns	Driver/API	SCPI / Python / QCoDeS
Analog bandwidth	215 MHz (-3 dB) 400 MHz (-9 dB)	Ethernet data rate	1 Gbit/s
Output range (in a 50 Ω load)	5 Vpp	Max. power consumption (via Cluster)	30 W
Rise/fall time (10%-90%)	< 1.4 ns	Analog Output connector type	SMA
THD (100 MHz, 1 Vpp in a 50 Ω load)	> - 65 dBc	Marker connector type	SMP
Voltage noise density (at 1 MHz in a 50 Ω load)	<7 nV/√Hz	Dimensions single module	269 x 130 x 20 mm³
Voltage noise density (at 1 Hz in a 50 Ω load)	1.0 µV/√Hz	Weight	0.295 kg