Introduction

All semiconductor process chambers need periodic cleaning and in high volume manufacturing deposition and etch, chambers are typically cleaned after a short run of wafers. For many common processes such as dielectric deposition (SiO_2 and Si_3N_4) chamber clean can happen as often as every 1-5 wafers and will typically represent 20% or more of the unit processing time. Build-up of material on the surface of the chamber from deposition or etch residue changes the characteristics of the process chamber and can lead to reduced process margin and yield crushing particulate materials. Making chamber clean a more efficient part of the semiconductor manufacturing unit process will have a significant positive effect on both throughput and process yield and is an overlooked part of fab and process operations.

The Problem

Much of the chamber clean activity in fabs today is fixed time-based cleaning where the chamber clean is run for a duration that is irrespective of the starting state of the chamber. Fixed time chamber clean is inherently inefficient, as excess clean time margin is required to ensure that all residues are removed. Clean time standard deviation from mean, dictates that typically 4 standard deviations (4 sigma) of clean time is required, resulting in consistent chamber over cleaning which has yield, environmental and throughput implications for the fab operator.

Why optimizing chamber clean is a win-win-win-win strategy

Overcleaning has multiple detrimental effects on fab operations:

- Throughput reduction due to longer than required clean time
- Throughput reduction and process gas use for chamber re-seasoning after over-clean
- Over-clean chamber damage (e.g. creation of AlF_3) resulting in particulate matter which effects yield
- Excess clean gas consumption and supporting abatement requirements

Optimizing clean is good for through-put, reduced consumables, higher yield and sustainability.

Sustainability is sharply in focus

While green energy use and water recycling efforts in FABs have made major impacts to scope 2 green-house gas emissions and water consumption metrics, the material portion of the semiconductor FAB sustainability challenge (scope 1 emissions) continues to grow as a percentage of the total. Finding pragmatic and easy to implement solutions is challenging for scope 1 materials emissions reduction. Optimized chamber clean reduces the amount of clean gasses that have to be abated. The most common chamber clean gasses are some of the worst greenhouse gas (GHG) contributors. Silicon Hexafluoride (SF_6), Nitrogen trifluoride (NF_3) and carbon tetra-floride (CF_4) are respectively 23,500x, 17,200x, and 6,500x more potent GHGs than carbon

dioxide and each has an atmospheric residency between of 1000's to 10,000's years longer than CO_2 - they are GHG pollutants that never go away. Reducing the use of these semiconductor clean gasses is a critically important and simple solution to significantly reducing scope 1 emissions from the worlds fabs.

Endpoint Based Clean Solutions Historically Challenging

In order to move from a timed based clean to an optimized end point detection-based process control solution, in-situ metrology is required that can work in the presence of the clean gases that are highly corrosive, present at high temperatures and produce particulate waste matter. Legacy metrology solutions such as optical emission spectroscopy (OES) and residual gas analysis (RGAs) are rendered ineffective in most applications of chamber clean. Poor OES instrumentation signal to noise ratio (SnR), low by-product residency times in the chamber, and process plasmas that are remotely generated, weak or not present all make optical emission spectroscopy ineffective for chamber clean monitoring. Likewise residual gas analyzers (RGAs) are not reliable as they suffer poor signal to noise ratio for measured clean byproducts, and from rapid deterioration of the ionizing filament in the presence of common clean glasses, with filament burn-out often measured in minutes.

The Solution

In a study on PECVD chamber cleaning end point detection (EPD) by Ho Jae Lee, Dongsun Seo, and Sang Jeen Hong from the Department of Electronic Engineering, Myongji University, Korea showed an average 53% reduction in clean time based on using EPD. However, EPD based time reduction from as little as 20% to as high as 63% over a dozen runs. The relatively high standard deviation of 10.8%, requires that continuous monitoring be deployed to achieve optimal and clean time. Extrapolating the data from Ho Jae Lee's paper we can estimate the true cost savings for a client running timed clean on a similar silicon oxide and nitride deposition process:

- In a recent case study at a client of Atonarp's the client was running timed chamber cleaning for 9 out of 45 minutes of unit process time, or exactly 20%.
- An average 53% reduction in clean time using EPD (as seen in the Myongji University paper) would save 10.6% in unit process time.
- Assuming an industry rule-of-thumb 82% tool up-time, the overall throughput benefit to the client would be approx 8.7% going from timed to EPD clean. (No savings from reduced or eliminated chamber seasoning is considered and would be incrementally beneficial).
- The higher unit process throughput can result in higher overall FAB wafer capacity, a reduction in wafer fab equipment CapEX for incremental capacity and a reduction in overall operating costs.
- A medium sized 40K wafer per month 300mm FAB with 8.7% incremental throughput can process an additional 3476 wafers a month worth over $10M at a $3K per 300mm wafer ASP, resulting in over $120M annualized incremental revenue.
- Reduction in clean gas consumption, high burn abatement fuel use and residual post abatement pollution of the process clean gasses is also an expected benefit both environmentally and in reduced sub-fab and material costs.

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Typical Return on Investment

Using cost effective in-situ metrology retrofitted on the chamber foreline exhaust allows for optimized clean time with very low risk to the existing process recipes and process qualification. ROI calculations vary from fab to fab and clearly will depend on the number of chambers and deployed metrology units required, but in most cases incremental cost savings and throughput enhancements result in an ROI period of 18 months or less.

Optimized chamber clean time requires robust, quantified, and real-time metrology fitted to the chamber exhaust forline. The Aston family of real-time semiconductor metrology solutions from Atonarp provide in-situ quantified metrology that is 10x to 100x better on the key sensitivity-at-speed metric than other residual gas analyzers with a robust plasma ionization solution that allows them to work with harsh process gasses and by-products even if process plasma is not available. Aston solutions uniquely have a high-performance hyperbolic quadrupole architecture that improves both x-axis and y-axis sensitivity for fast accurate and highly sensitive endpoint detection in semiconductor applications.

Proof of concept (PoC) activities at a number of clients have resulted in significant chamber clean time reductions (up to 75%) using Aston for EPD. The PoCs have also demonstrated the requirement for continuous monitoring based on variable chamber clean requirements in order to consistently optimize clean time.

Summary

Aston's advanced molecular profiling with a speed/sensitivity capability that is 10x to 100x better than legacy metrology and is enabling advanced chamber clean optimization to improve throughput, consumable consumption and sustainability with a rapid ROI on the cost of deployed units.