Husna Kalim

Electrical and Computer Engineering Student, UBC

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SKILLS

Technology: Digital system, Microwave technology, Sub-System and System Level testing.

Test Equipment/Platform: Spectrum Analyser, SigGen, Multimeter, CRO, FPGA, Microcontrollers, Microprocessors. **Programming/Software tools:** C, Python, VHDL, Xilinx, Quartus, Altium, SAP, Microsoft Office.

EDUCATION

University of British Columbia, Vancouver	01/2021 – present
Master of Engineering, Electrical and Computer Engineering	
Sauder School of Business, UBC	11/2021 – 04/2022
Tech Entrepreneurship course	
Visvesvaraya Technological University	09/2010 – 06/2014
Bachelor of Engineering, Electronics and Communication Engineering	

WORK EXPERIENCE

BHARAT ELECTRONICS LIMITED, Deputy Engineer (System Test Engineer)

05/2015 - 01/2021

05/2022 - 12/2022

• Responsibilities

- Execution of RF Design and testing of C-band Super Heterodyne Receiver and Exciter Unit.
- Test digital systems and modules using best practices and provide product validation reports.
- Define, implement, verify and validate test plans.
- Contribute and manage overall hardware system requirements.
- Audit AS 9100 Rev D Standards as a certified department member and status reporting with 5S implementation.
- Supervise and conduct four training sessions for a batch of 65 users annually.
- Working closely with cross-functional teams.

Achievements

- Performed CA PA (Corrective and Preventive action) analysis of failed modules at the field level and reduced dependency to 50%.
- Reduced product failures to 2% by conducting environmental stress screening of PCB's and RF modules.
- Documented test procedures in the form of a flowchart for easy analysis to debug and bring up the system.
- Qualified 12 sub systems as per Military Grade JS55555 standard within a month.
- Received recognition from General Manager and awarded with "Young Achievers for Executives Award".

MICROCHIP TECHNOLOGY Product Engineer Co-op

- Responsibilities
 - Performed characterization experiments on mixed-signal and high-speed semiconductor devices.
 - Developed custom test hardware and test programs for high-volume production testing.
 - Performed functional analysis of PCIe Gen1, Gen2, and Gen4 high-speed switch based on NRZ SerDes.

Achievements

- Optimized the script to test and export the data for data pipelining and data analysis.
- Completed PCIe Gen 1 and Gen 2 characterization by reducing the test duration.

LEADERSHIP AND INVOLVEMENT

- I mentor underprivileged students and help them with personal and academic development.
- Volunteered in 1st-year Orientation event and organized Welcome back event for 2nd year ECE students at UBC.
- Involved in outdoor activities and hikes, to plant more trees as a gesture of gratitude, and to care for animals.

ATTACHMENT

Attachment-1 Project Details

Project Details

1. Gen 4 PCIe Switch Validation, Microchip Technology

- Role: Product Engineer Coop
- Description: Characterization of the Gen 4 (16Ghz) PCIe switch involves initialization and calibration to configure all the analog circuits, based on the request from the interface. We configure the clocking system unit with different clocking architectures for Gen 3/4/5, then run the receive adaptation to assert RX valid and perform a Link equalization test before firmware servicing requests like capturing eye diagram.
- Responsibilities:
 - o Acquiring a high-level conceptualization of the Validation needs
 - \circ $\,$ Collaborating with the design team to upgrade the firmware of the device
 - \circ ~ Use JBERT to calibrate the test setup and confirm the device operating requirements.
 - Evaluate performance with common clock architecture with additional impairments.
 - Create Python scripts to modify devices and evaluate jitter tolerance.
 - Examine the performance of NRZ-based SerDes, 100-lane switch for PVT conditions at all process corners.
 - Improve the performance of the device by setting the ideal parameters.

2. Gen 1/2 PCIe Switch Validation, Microchip Technology

- Role: Product Engineer Coop
- Description: Characterization of the Gen 1 (2.5Ghz) and Gen 2 (5Ghz) PCIe switch involves initialization and calibration to configure all the analog circuits, based on the request from the interface. We configure the clocking system unit with different clocking architectures (CC, SSC, SRNS) for Gen 1/2, then run the receive adaptation to assert RX valid and perform a Link equalization test before firmware servicing requests like capturing eye diagram.
- Responsibilities:
 - o Acquiring a high-level conceptualization of the Validation needs
 - \circ $\;$ Collaborating with the design team to upgrade the firmware of the device
 - \circ ~ Use JBERT to calibrate the test setup and confirm the device operating requirements.
 - Create Python scripts to modify devices and evaluate jitter tolerance.
 - Examine the performance of NRZ-based SerDes, 100-lane switch for PVT conditions at all process corners.
 - \circ $\;$ Improve the performance of the device by setting the ideal parameters.

3.TxRx Impedance Calibration, Microchip Technology

- Role: Product Engineer Coop
- Description: The analog test bus is connected to different blocks of transmitter and receiver; impedance mismatch can lead to signal reflection and cause interference that deteriorates the jitter tolerance at the receiver and causes jitter attenuation problems at the transmitter. In this project, I configured the registers and implemented a firmware doorbell function that asserts one block at a time and contributes to the consistent voltage on the analog test bus.
- Responsibilities:
 - Arrange setup to test voltage after enabling various blocks.
 - Find the underlying cause of the impedance mismatch and voltage variation on the power rails by performing all feasible tests and repeating them 1,000 times to identify any device repeatability problems.
 - o Identify the registers and create a Python calibration script.

4. Radar Receiver (Radar Subsystem), Bharat Electronics Limited

- Role: System Engineer
- Description: In Radars receiver amplify and demodulate the received RF signals, the received RF signals must be transformed into a video signal to get the wanted information from the echoes. This transformation is made by a superheterodyne receiver. The Receiver Exciter operating in the C band (4 to 8 GHz) frequency range is tested for double-down conversion and generation of accurate timing signals and reference clocks that drive the clocking of Radar.
- Responsibilities:

- Creating a product specification, getting consumer feedback on the design, developing a simulation for product testing, and information transfer.
- Create a test setup for the P1 dB compression test, the stable multiple oscillator output test, and the receiver gain test.
- o Examining the design and offering comments
- Provide new hires with technical and soft skill training

5. Road Deterioration Detection Deep Learning Project, UBC

- Role: Student
- Description: Road Deterioration Detection project using Deep Learning techniques. Based on the data collected, this connected car technology will allow a vehicle to gather data about the location and severity of potholes, allowing the driver to slow down the car or adjust its suspension settings to reduce the impact and smooth the ride, to reduce the potential for punctures, and vehicle damage. This project relates to the Personalised Learning and Assessment team because it depends on computational cognitive modelling and predicting the outcomes through usage data.
- Responsibilities:
 - Visualize data; the video of the road's surface had to be turned into frames.
 - Using Computer Vision Annotation Tool, the 27,293 frames were labelled and annotated using bounding boxes.
 - \circ Created a high-accuracy road detection method utilizing machine learning techniques.
 - Setting up scripts to find mal learning rates, and test performance with different hyper-parameter values which include experimental runs with different weighing regularizes, changes in loss functions and activation functions.
 - Built a deep neural network with YoloX, Swin transformer, Adam, and SGD optimizer.

6. Radar Scan Converter (Positioning Radar Subsystem), Bharat Electronics Limited

- Role: System Test Engineer
- Description: The receiver down-converts the radar waveforms from RF to IF and sends them to the processing unit after down-converting to IF for further processing and producing the desired output. The Radar scan converter extracts the information and displays the salient characteristics of target echo, strength variations, Doppler phase shift, angle error, etc.
- Responsibilities:
 - Comprehending the design requirements and envisioning them in high-level detail.
 - \circ $\;$ Scheduling the design and development process across the design life cycle.
 - Reviewing the design to offer comments after my team members' work on the schematic design, integration, and review.
 - Provide new hires with technical and soft skill training.

7. TECH E Project, Sauder School of Business

- Role: Technical Engineering Consultant
- Description: The objective of the Tech-E project was to come up with a better solution for an existing problem. In the cold storage industry, current gas detectors used in practice are expensive and can only detect one gas per sensor, The better solution was to provide a novel comprehensive cold storage gas monitoring system which can detect multiple gases in a single detector device, real-time data analysis and smart features like communicating with a mobile system.
- Responsibilities:
 - Extensive Market survey of the existing solutions and their problems, new requirements from the customer, sourcing, and security concerns.
 - Architecting and building the prototype, costing, and optimizing the total cost of manufacturing.
 - Plan the maintenance of the device post-manufacturing.