



Power Management Integration Center

Hybrid-Resonant Switched Capacitor Converters: Topologies, Trends, and Challenges

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Power Management Integration Center PMIC



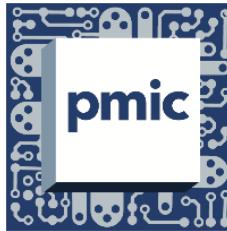
Power Management
Integration Center

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ENGINEERING
AT DARTMOUTH



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Power Management Integration Center

<https://pmic.engineering.dartmouth.edu/>

- National Science Foundation (NSF): **Industry/University Cooperative Research Center (I/UCRC)**
- **Focus: higher efficiency, smaller size, and reduced cost in power electronics**
- Funding model for Industry-Driven University Research @ Dartmouth and UC San Diego center sites
- Company Membership
 - Access to IP, students, faculty
 - Select research projects
 - Two annual meetings, monthly updates
- Next IAB Meeting June 27 & 28
- Contact: pmic@thayer.dartmouth.edu



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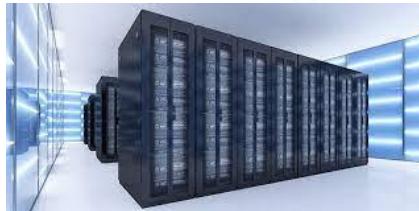
Important Areas in Power Management

Application

Mobile Devices & Communication



Performance Computing



Renewable Energy,
Automotive



IOT/Wearables/COTS
Robotics



Trends

Pressure on battery life,
size, cost, functions



cores, density,
integration, parasitics



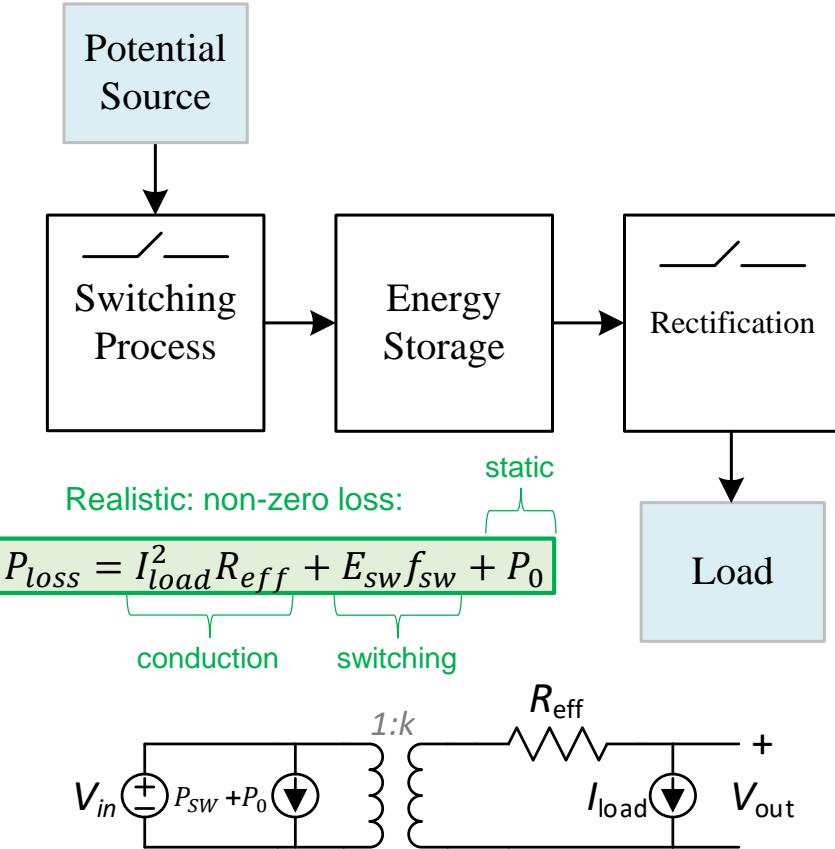
Extreme cost pressure,
reliability, multi-function



Extreme low power,
size and cost



DC-DC Abstraction



Efficiency Considerations:

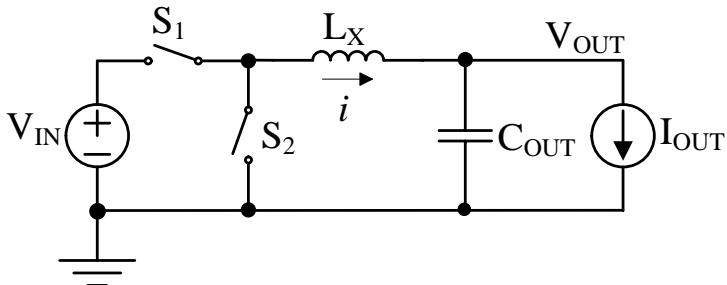
- Resistance (conduction loss)
- Frequency dependent losses
- Passive component losses



Density Considerations:

- Energy density (passives)
- Frequency (how much energy storage?)
- Utilization (passives)

High Density Power Conversion



→ Reduce passive component volume

- Strategy 1: **Increase frequency**
 - + **Good:** Smaller inductor, capacitor
 - **Bad:** Increase in frequency dependent losses (winding, core, gate drive etc.)

$$\Delta i_{pp} \propto \frac{\Delta V}{f_{sw} L} \left[\frac{V \cdot s}{H} \right]$$

$$\Delta v_{out,pp} \propto \frac{\Delta i_{pp}}{f_{sw} C_{out}} \left[\frac{A \cdot s}{F} \right]$$

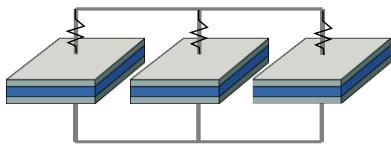
- Strategy 2: **Change Architecture**
 - Reduce inductor ΔV
 - Reduce output cap ΔI
 - Multiply 'effective' frequency

Better Utilization

Passive Component Density Considerations

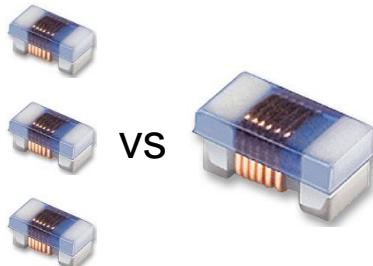
- Capacitors → **higher energy density** than inductors
- Always better with ‘**physically larger**’ magnetic components

Capacitors



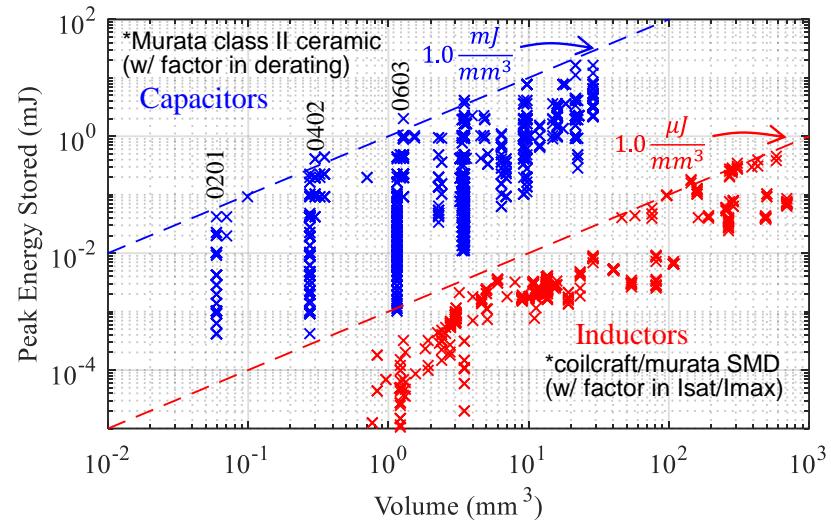
$$Q \propto \frac{1}{RC} \approx \text{constant}$$

Inductors



$$Q \propto \frac{L}{R} \approx \text{Volume}^{\alpha}$$

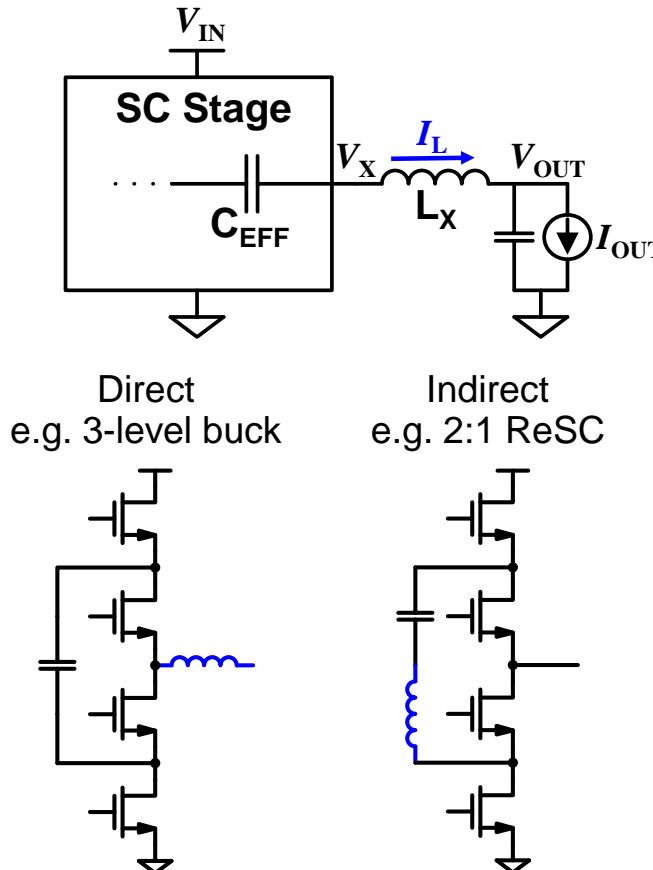
$\alpha \sim 2/3$ (or at least > 0)



[Sullivan et al., “On size and magnetics: Why small efficient power inductors are rare,” 3D-PEIM, 2016]

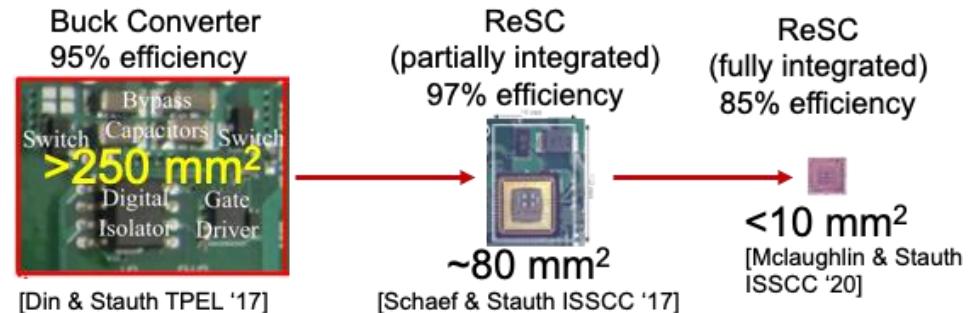
[Kyaw & Sullivan et al., “Fundamental Examination of Multiple Potential Passive Component..,” TPEL ’18]

Hybrid/Resonant SC Converters



Switched Capacitor Stage + Inductor(s)

- Leverage **high energy density** SC network
 - Reduce inductor ΔV
 - **Reduce inductor energy storage and size**
- Inductor → **eliminate ‘charge sharing’** in SC stage
 - **Higher efficiency** (lower cond. loss and sw. frequency)
 - **Higher power density** (smaller passive component volume, better utilization of semiconductor devices)



Past and Future

Many examples in past literature:

[Cuk/Middlebrook, Meynard, Maksimovic, Nishijima, Sanders, Prodic, Pilawa, Stauth, H.P. Le, Mercier, Ruderman, F.Z. Peng, Peretz, Evzelman, Smedley, S. Jiang, Shenoy, Ioinovici, B. Wicht, Trescases, many others...]

Middlebrook, "Transformerless DC-DC Converters with Large Conversion Ratios," TPEL '88]

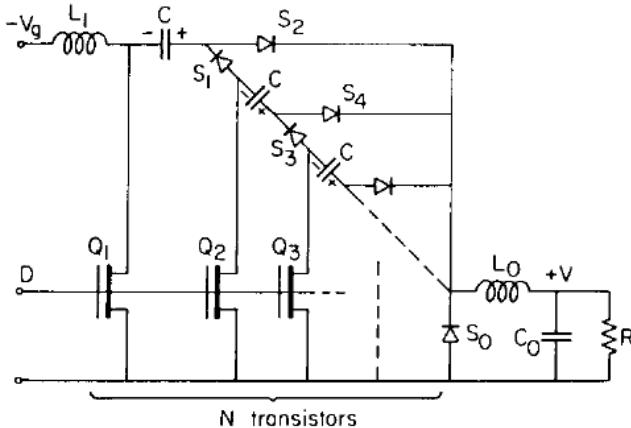


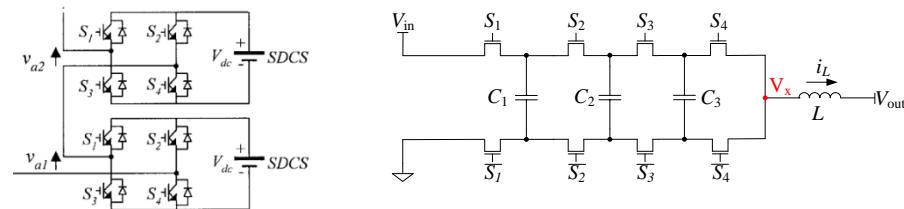
Fig. 3. Generalized N -stage voltage-divider Ćuk converter.

Where these concepts are already mainstream:

- High voltage MMC, HVDC, etc
- Switch/Component voltage ratings << app. spec

[MMC: Tolbert et al., many others]

[FCML: Meynard et al., many others]

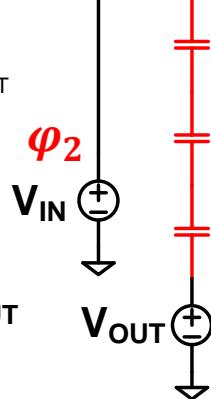
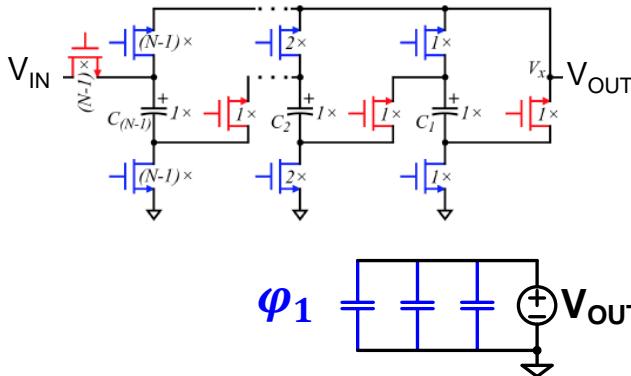


Why now and going forward:

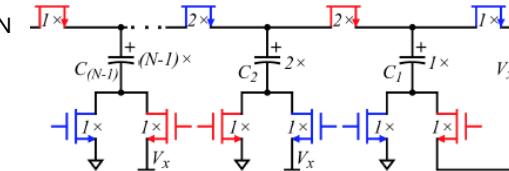
- Switch/Component voltage ratings << app. spec (better overall utilization of semi devices, passives)
- Integration allows new topologies/architectures (many more switches, capacitors)
- New passive components (high density cap)
- New integration platforms (interposer etc.)

Switched Capacitor ‘Base’ Classes

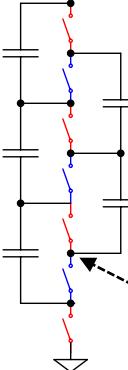
Series Parallel



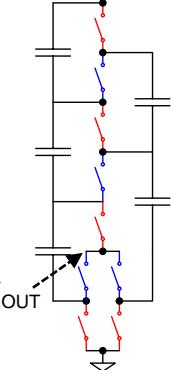
Dickson/Ladder/CW



Ladder



Cockcroft Walton



Perspective:

- Min cap (dielectric) volume to block $V_{IN}-V_{OUT}$
- ..But requires switches to absorb high voltage stress

- **Best capacitor (passive) utilization**
- Worst switch utilization



Perspective:

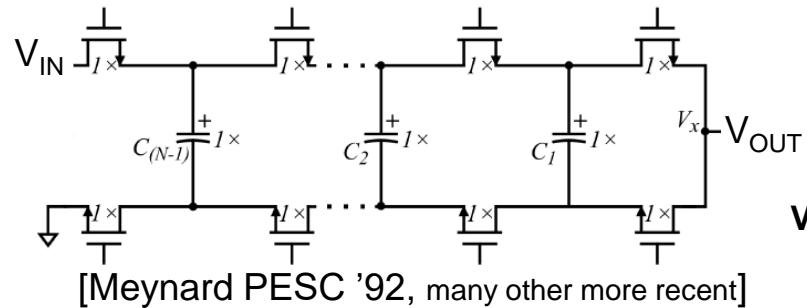
- Min switch rating (area etc.) to block $V_{IN}-V_{OUT}$
- ..But requires capacitors to absorb high voltage stress

- Worst capacitor (passive) utilization
- **Best switch (active) utilization**

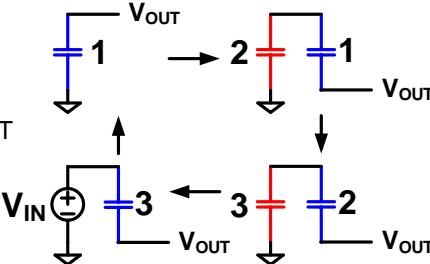
Other Common Examples

Flying Capacitor Multilevel FCML

aka 'multilevel buck'

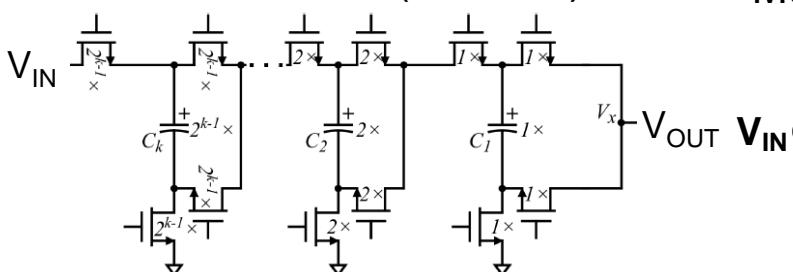


Multiphase operation

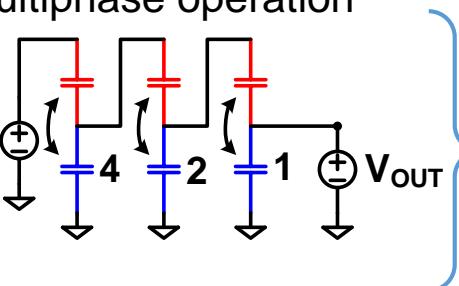


- Dickson-like charge multiplier
- Intermediate utilization
- **Multilevel = diff't VCRs**
- **Effective fsw multiple.**

Cascaded (doubler)



Multiphase operation



[Ye et al., "The Cascaded Resonant Converter..." TPEL '20]

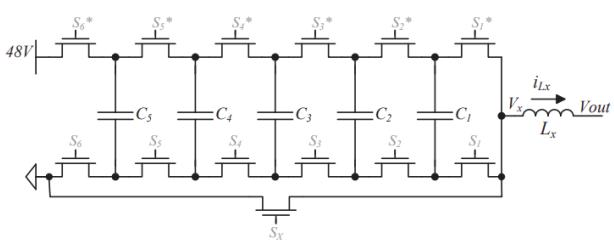
[Xia & Stauth, "A Two-Stage Cascaded Hybrid Switched-Capacitor..." ISSCC '21]

@multiphase operation:

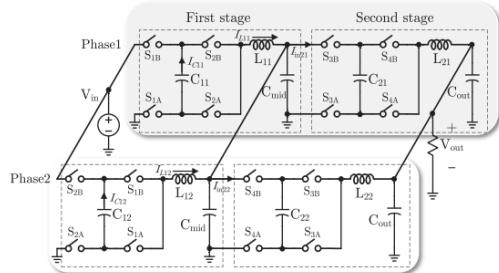
- Intermediate utilization
- **Highest VCR per cap of 'any' SC topology**

Example Topologies, Discrete

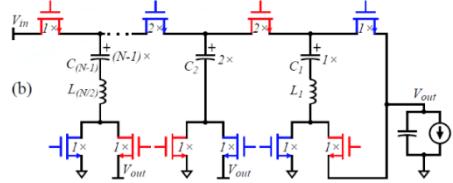
48V:2V FCML
w/ Valley-Current Control
[Rentmeister & Stauth APEC '17]



Cascaded Resonant Converter
[Ye & Pilawa, TPEL '20]

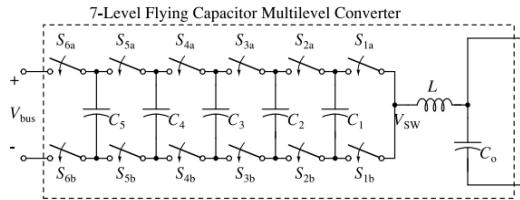


'Switched Tank'
[Jiang et al., TPEL '19]
'indirect' resonant
Dickson topology



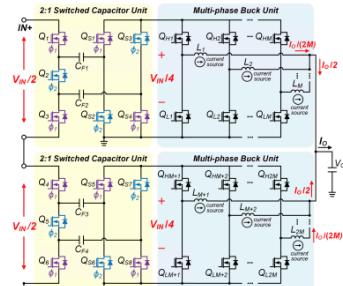
- 48:12V step down
- Over 98% peak eff.
- Over 500W/in²

FCML Inverter (LittleBox)
[Lei et al. & Pilawa, TPEL '17]

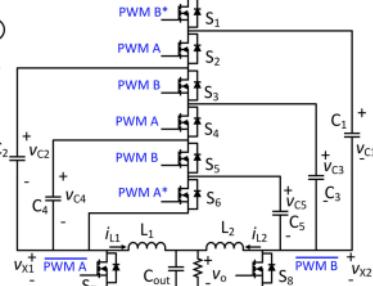


- 2kW Multilevel inverter
- 97.6% eff @ >200W/in³
- Active energy buffer

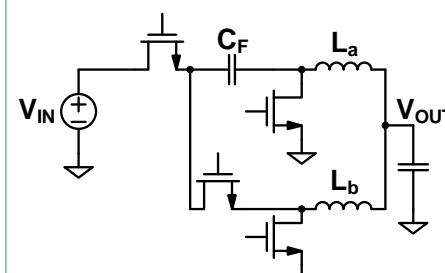
Lego-PoL: high VCR
[Baek & Chen '19-'21]



Dual-Inductor Hybrid
[Seo/Das & HP. Le '19-'21]



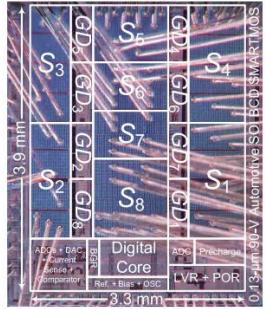
DSD/Series Cap Buck
[Nishijima '05; Shenoy '15]



Example Topologies, Integrated

Automotive-Grade 48V Dickson

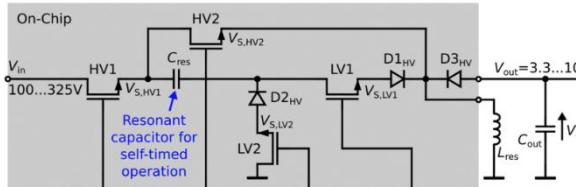
[Asherloo et al., & Trescases ISS/JSSC '21]



- 48V: \sim 3.3V step down @ 91.4% efficiency
- Startup pre-charge, fault det.
- Valley current balancing
- Masterless multiphase

HV Self-Timed Resonant DC-DC

[Rindfleisch & Wicht ISSCC '20]

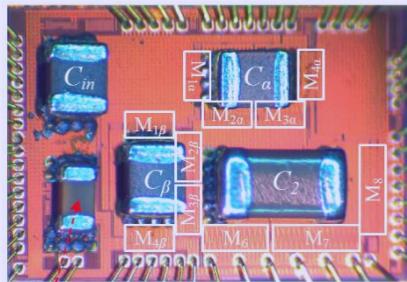


- **High Voltage!** 325V: \sim 3.3V step down @ 50-60% efficiency (quite good!)
- On-chip HV resonant capacitor
- Self-timed ZVS/ZCS!

Cascaded Step Down Converter

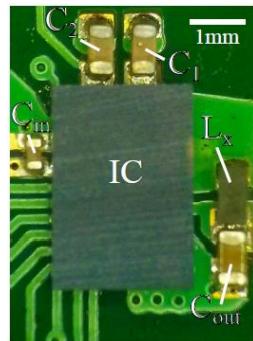
[Xia et al., ISSCC '21]

- High VCR \rightarrow 5V:0.4-1V @ 96.9% efficiency
- Startup in $<10\mu\text{s}$
- Nonlinear control: Fast load transient & flying capacitor balancing



Quasi-resonant Series Parallel

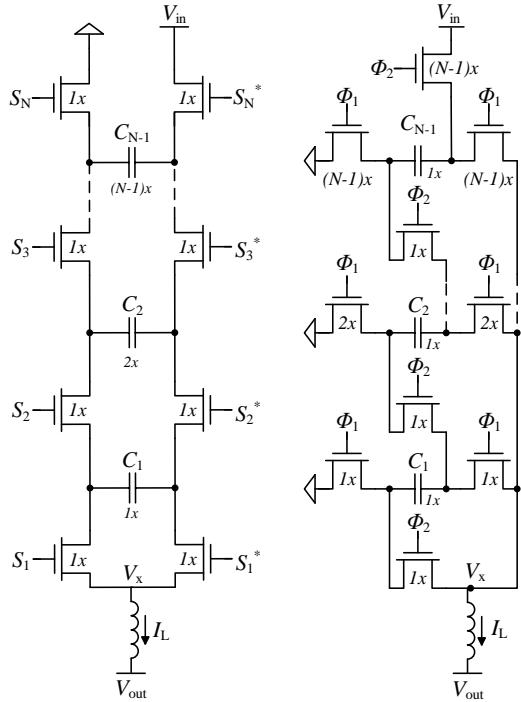
[Schaef et al., JESTPE '17]



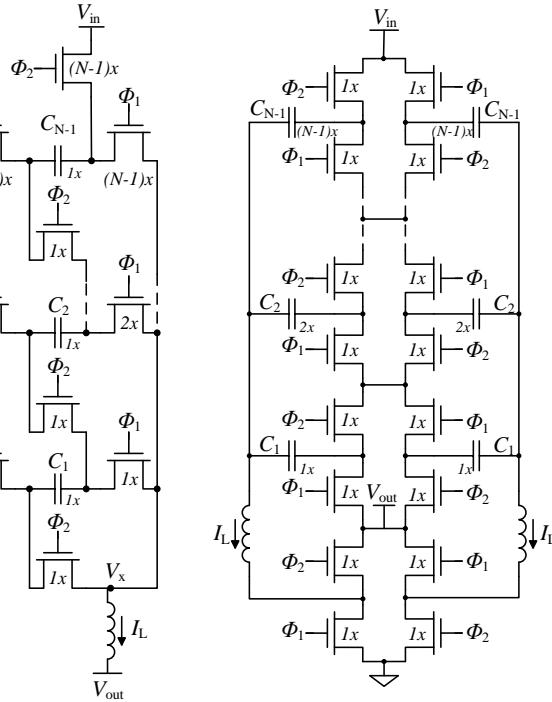
- Early demonstration of startup pre-charge circuit, ZVS method
- 33nH inductor
- 330nF flying cap
- 12V:3.7V, 4.6W at 87% efficiency

Topology Comparison

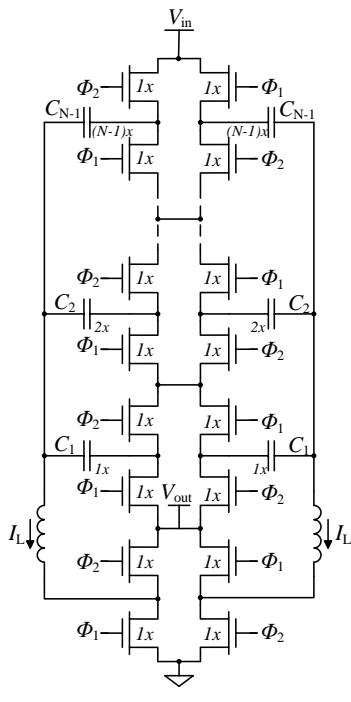
Many possible hybrid-SC topologies, Which is best?



Series Parallel
(Direct)



Dickson
(Indirect)



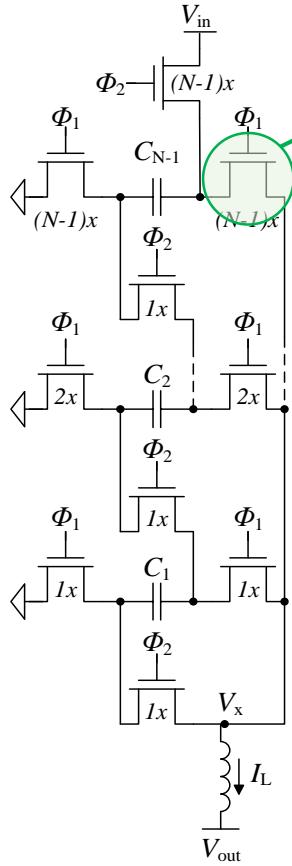
- Active device utilization?
- Passive component utilization?
- Other considerations?

Exercise: Pasternak, Kiani, McLaughlin
[Compel '17,'18; TPEL '21]

- Minimum power loss FOM
(active devices and inductor)
- Size constraints on passive components

[McLaughlin et al., “Analysis and Comparison of Hybrid-Resonant Switched-Capacitor DC–DC Converters With Passive Component Size Constraints,” TPEL ’21]

Minimum Power Loss FOM Development



Arbitrary device, loaded with I_{rms} , operating at f_{sw}

$$P_{sw} = I_{rms}^2 R_{on} + f_{sw} E_{sw} + P_{extra}$$

Size-dependent specific parameters:

$$R_{on} = R_{sp} / S$$

$$E_{sw} = E_{sp} \cdot S$$

S Area
Volume
Width
Weight

$$\frac{dP_{sw}}{dS} = 0$$

Well-known minimization:

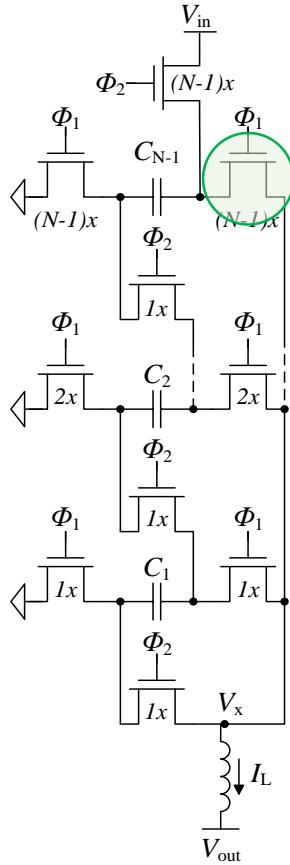
$$P_{min,sw}^* = 2I_{rms} \sqrt{f_{sw} R_{sp} E_{sp}}$$

Sum across all devices:

Explore this next

$$P_{total,switches}^* = 2\sqrt{f_{sw}} \sum_{i \in switches} I_{rms,i} \sqrt{R_{sp,i} E_{sp,i}}$$

Minimum Power Loss FOM Development



$$P_{total, switches}^* = 2\sqrt{f_{sw}} \sum_{i \in switches} I_{rms,i} \sqrt{R_{sp,i} E_{sp,i}}$$

General Scaling: $\propto v_{r,i}^\alpha$

$$I_{rms,i} = \beta_{r,i} \alpha_{r,i} I_{out}$$

RMS/DC ratio in switch

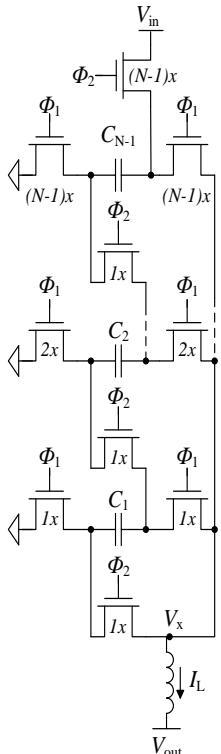
Total DC output current (load)

Charge multiplier: Fraction of total output current that flows in switch

$\alpha \approx 3$	CMOS (constant field)
$\alpha \approx 2$	CMOS (cascode)
$0 < \alpha < 2$	GaN, SiC, Discrete Si

@ $\alpha = 0 \rightarrow$ All devices same rating

Comparison Development: minimum power loss in arbitrary dc-dc converter



[Kiani & Stauth, “Optimization and comparison of hybrid-resonant switched capacitor...” COMPEL 2017]

$$P_{SW}^* = 2I_{out} \sqrt{R_{sp0} E_{sp0}} \times \sqrt{f_{sw}} \sum_{i \in switches} \beta_{r,i} a_{r,i} v_{r,i}^{\alpha/2}$$

Invariant/normalized

Topology specific FOM

Explore This Next

Comparison Development: minimum power loss in arbitrary dc-dc converter

Active device utilization:

@Same VCR, I_{load} , f_{sw} : Topology with lowest $\sum \beta \alpha v$ achieves lower loss; better use of available semiconductor Rsp*Esp

$$P_{SW}^* \propto \sqrt{f_{sw}} \sum_{i \in switches} \beta_{r,i} a_{r,i} v_{r,i}^{\alpha/2}$$

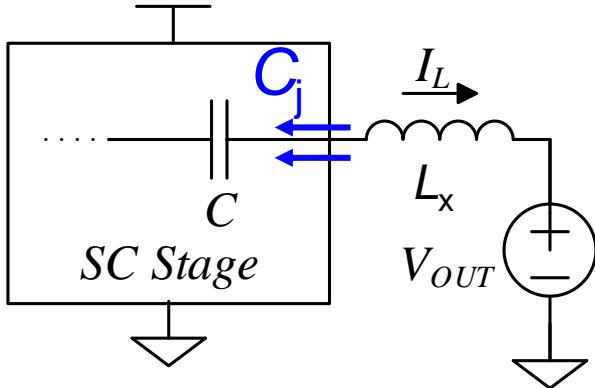
Note: @ $\beta = 1$; $\alpha = 2$, this is same as common $\sum AV$ comparison

Passive Component Utilization

Assume same total energy, area, volume, voltage/current ripple limit, etc

@Same total passive component size: Deliver more energy/cycle or same **same I_{load} at lower f_{sw}** → better use of available passive energy

Resonant Frequency as Proxy $\sqrt{f_{sw}}$

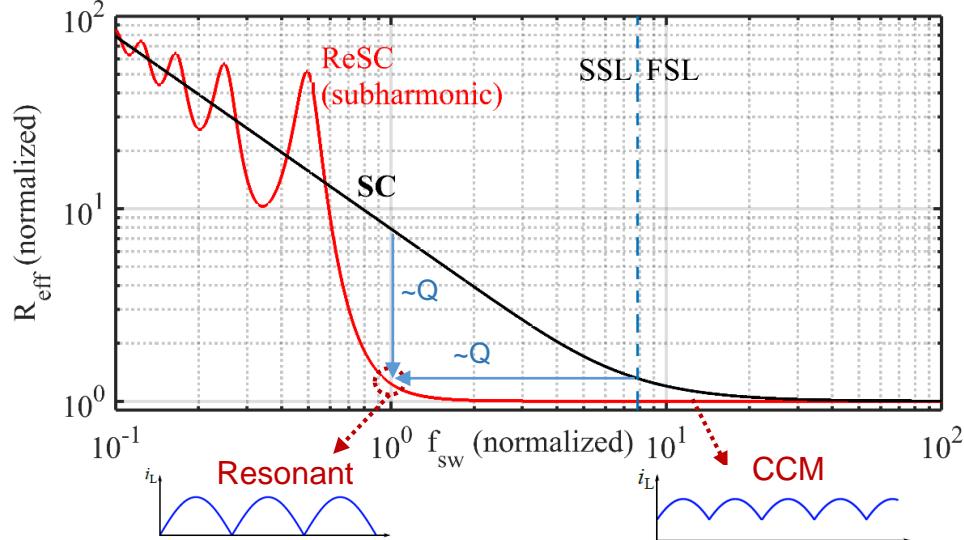


Hybrid topologies:

*Resonant/Critical frequency:

Sets lower limit for operation

$$f_{sw} = \frac{1}{\pi \sqrt{L_x} \cdot \sum_{j \in \text{phases}} \sqrt{C_j}}$$



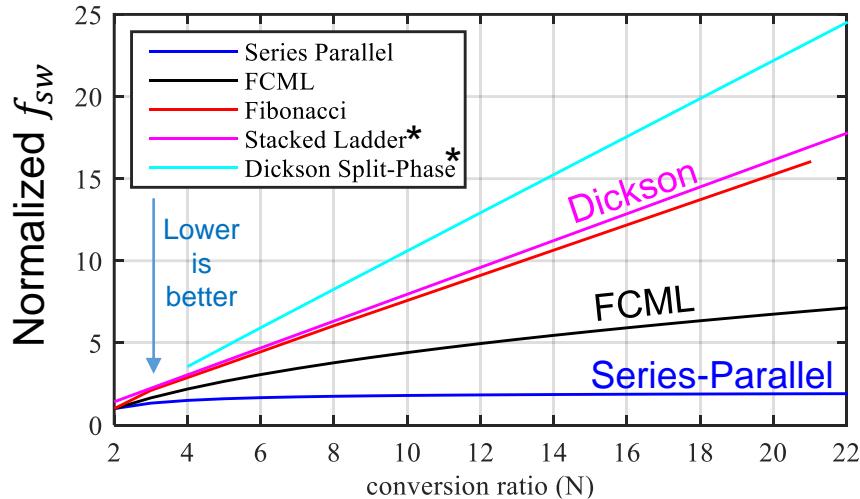
Topology that presents **higher 'Thevenin eq.' capacitance** across phases \rightarrow **lower frequency**
 \rightarrow Same I_{LOAD} , lower f_{sw} \rightarrow higher utilization

Active and Passive Component Utilization

~similar to MSSL and MFSL metrics in [Seeman TPEL '08]

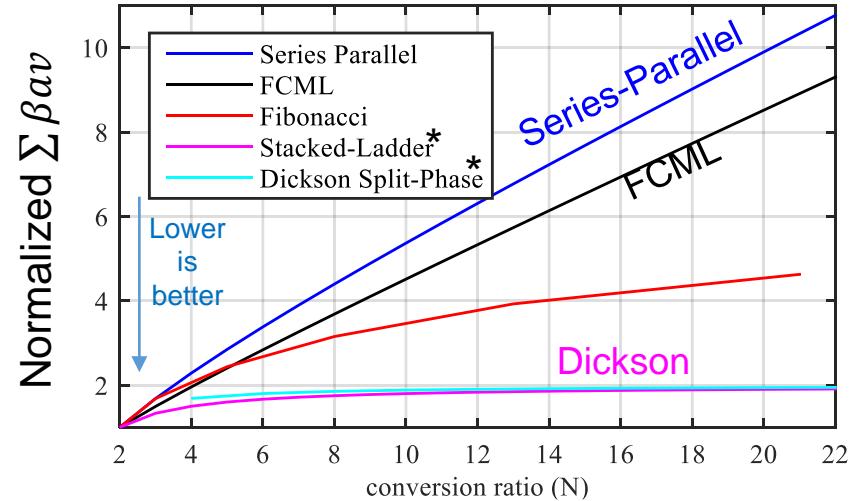
Passive Component Utilization:

Fixed Total Cap Volume, same L



- Competing 'dual' advantages:
- Dickson has better use of switches
- SP has better use of Capacitors

Device Utilization: $\sum \beta av$



*Dickson Topologies: 1. Split Phase Dickson: [Lei & Pilawa, TPEL '16]
2. Stacked Ladder: [Li & Sanders, ECCE '16]

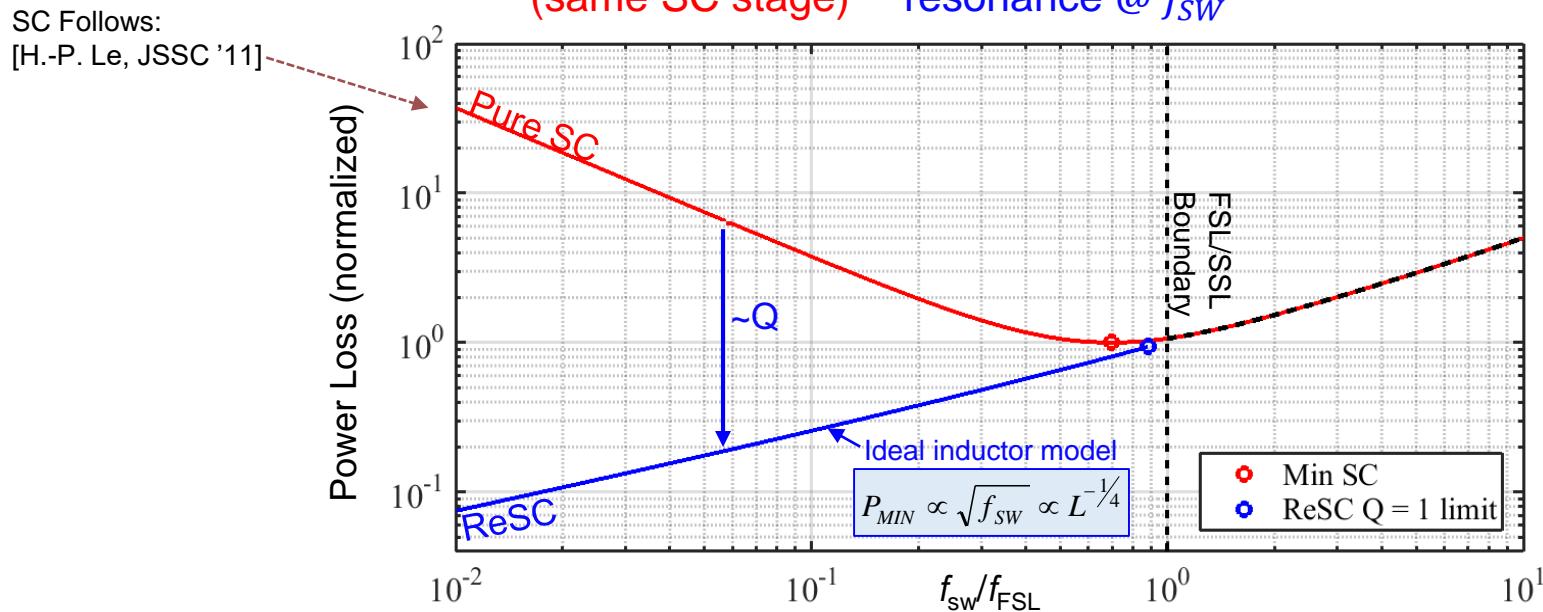
**Still need to factor in inductor;
Combine metrics for full perspective**

Combining Inductor Losses, Consider Inductor Sizing

Note: switches everywhere optimized (min loss @ each f_{sw})

$$P_{total}^* \propto \frac{1}{(C_{EFF}^* L)^{1/4}} \sum \beta_{r,i} a_{r,i} v_{r,i}$$

C_{EFF}^* = fixed
(same SC stage) L = scaling for resonance @ f_{SW}



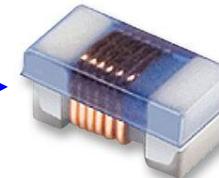
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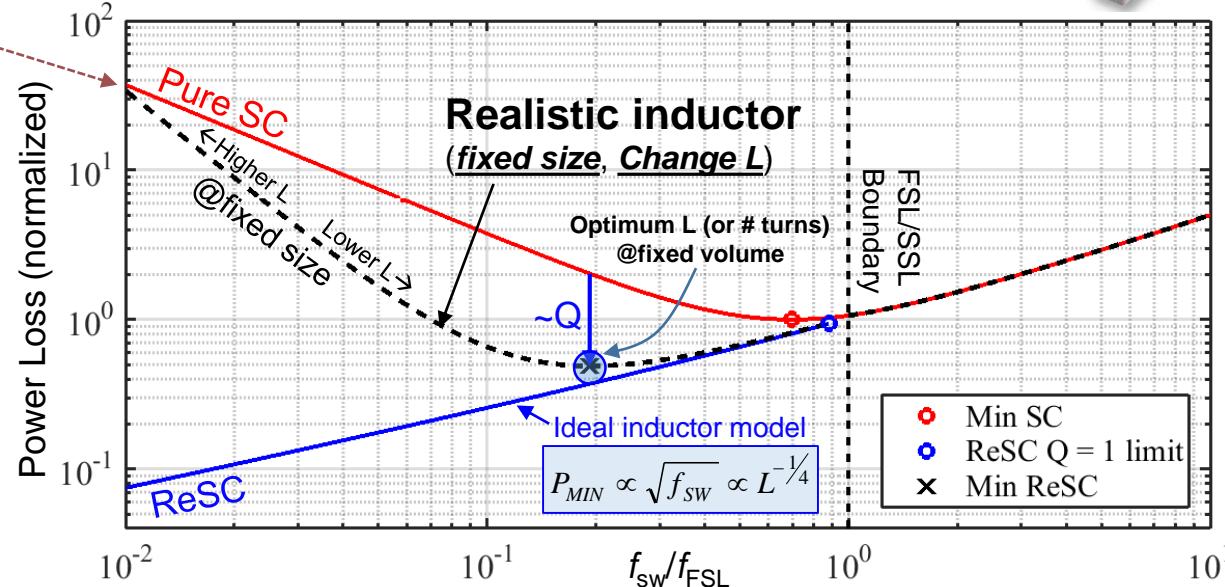
L = scaling for resonance @ f_{sw}



[Scaling Laws: Perreault et al and Sullivan, APEC '09]

@ fixed volume, scale # turns, **fixed L/R ratio**

SC Follows:
[H.-P. Le, JSSC '11]



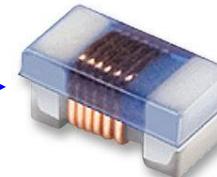
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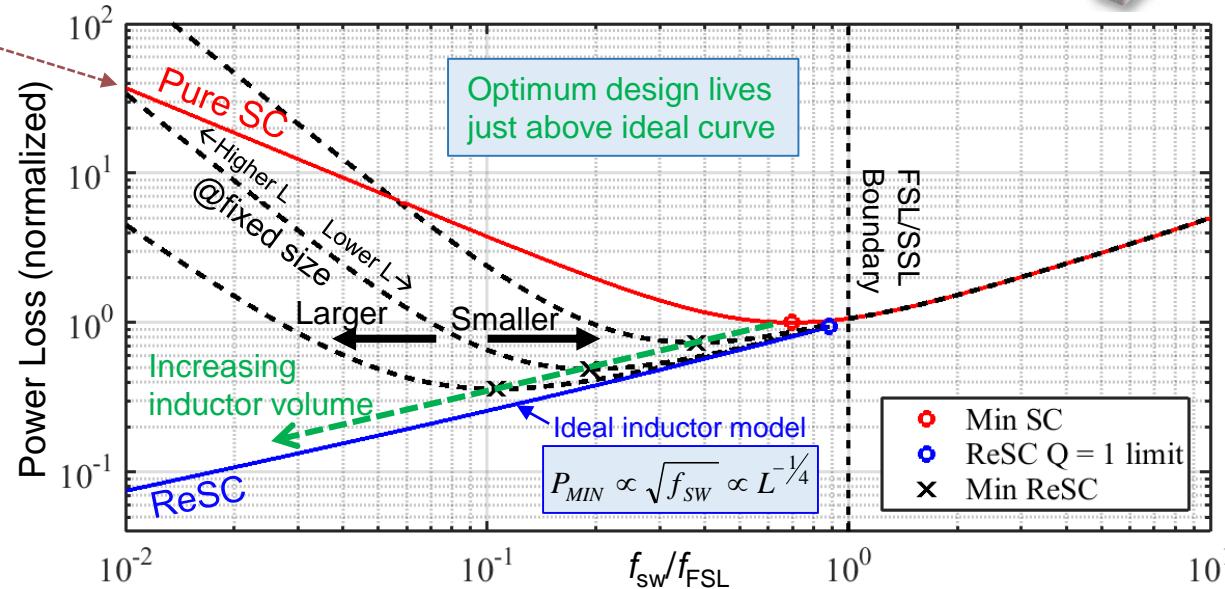
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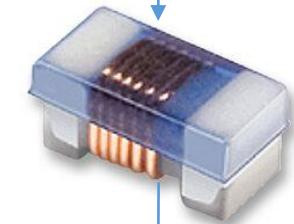
SC Follows:
[H.-P. Le, JSSC '11]



@ fixed volume, scale # turns, **fixed L/R ratio**



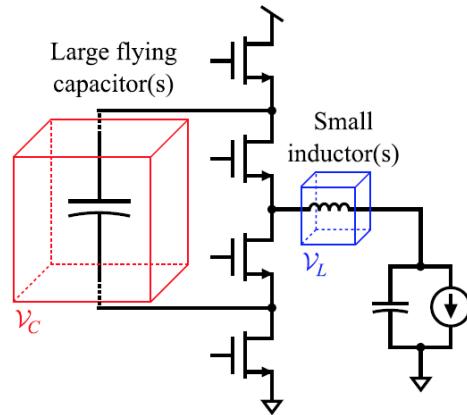
Smaller = Lower L/R



Larger = Higher L/R

@ Fixed Total Passive Component Size

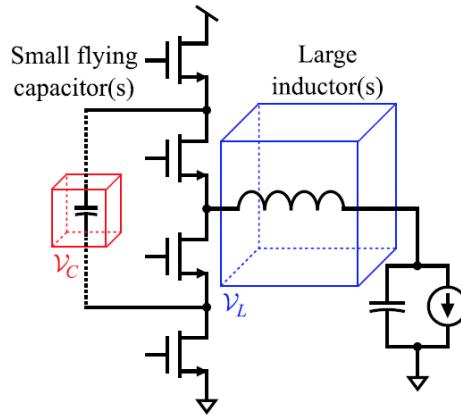
@Large C, Small L:



More loss in L

Optimum L
@ diff't size

@Large L, Small C:



Lower loss in L

Consider effect on
overall circuit losses

Optimal Sizing

[Kiani COMPEL '18]

[McLaughlin TPEL '21]



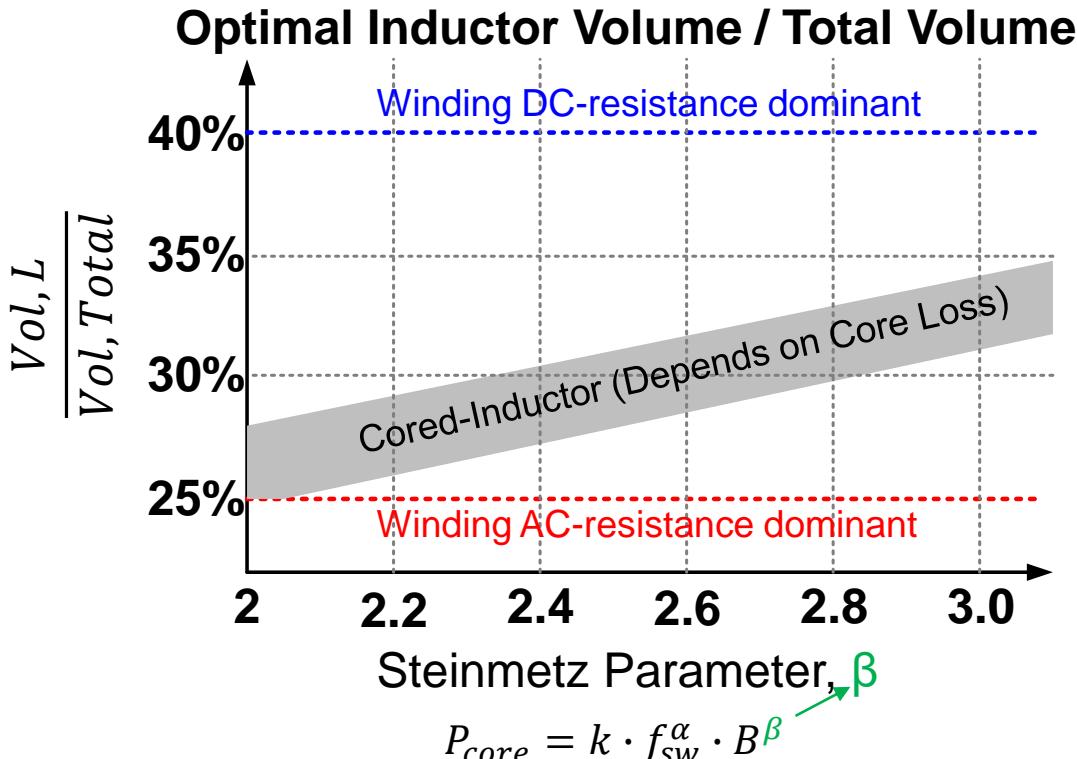
- Minimum total loss
- Generally minimizes f_{sw}

[McLaughlin, et al., "Analysis and Comparison of Hybrid-Resonant Switched-Capacitor DC-DC Converters With Passive Component Size Constraints," TPEL '21]

Assume Fixed Total Passive Component Size

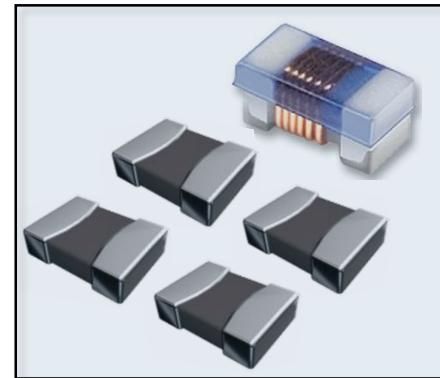
Takeaway: Inductor is ~25% to ~40% of total Volume

Depends on 'how losses scale:' DC & AC resistance, core loss etc.



Optimal Sizing

[Kiani COMPEL '18]
[McLaughlin TPEL '21]

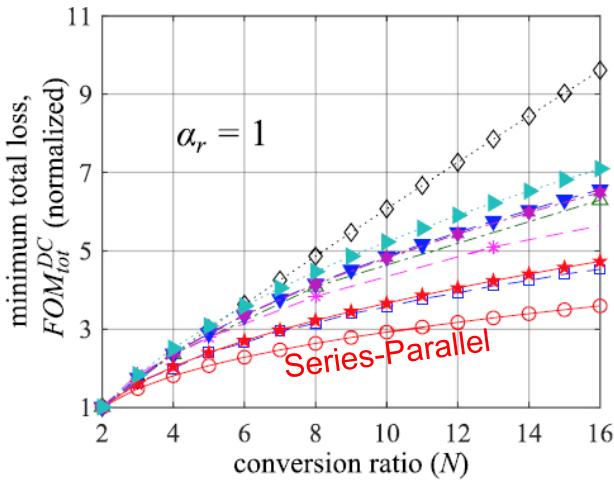


- Minimum total loss
- Generally minimizes f_{sw}

Topology Comparison (Fixed Passive Volume)

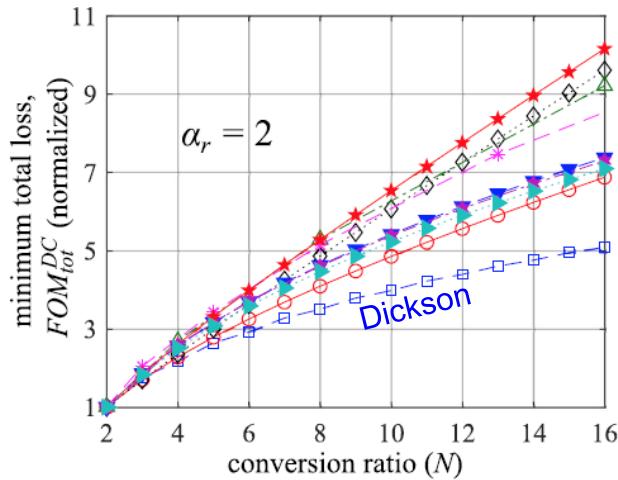
Inductor DC resistance loss model

— □ — Ideal Dickson	— ○ — Series-Parallel	··· ♦ ··· FCML	— * — Fibonacci	— ▲ — Casc. Doubler
— ▼ — Dickson (Multi-L)	— * — Sw. Tank (Multi-L)	— ★ — Series-Parallel (Multi-L)	— ▶ — Ladder (Multi-L)	



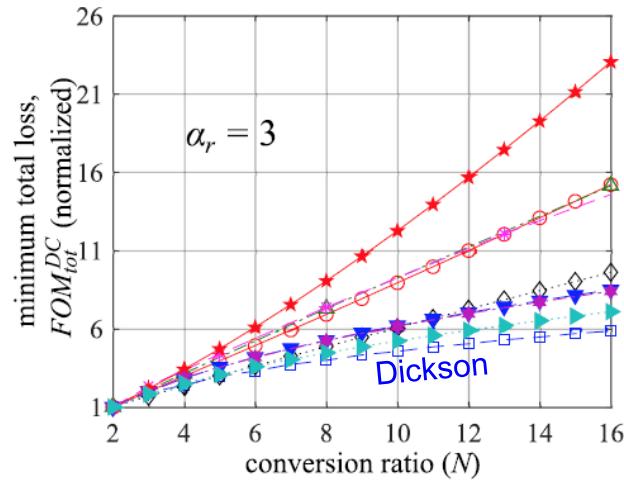
$\alpha_r = 1$
(GaN/SiC etc.)

← Series Parallel Better



$\alpha_r = 2$
(Cascode scaling)

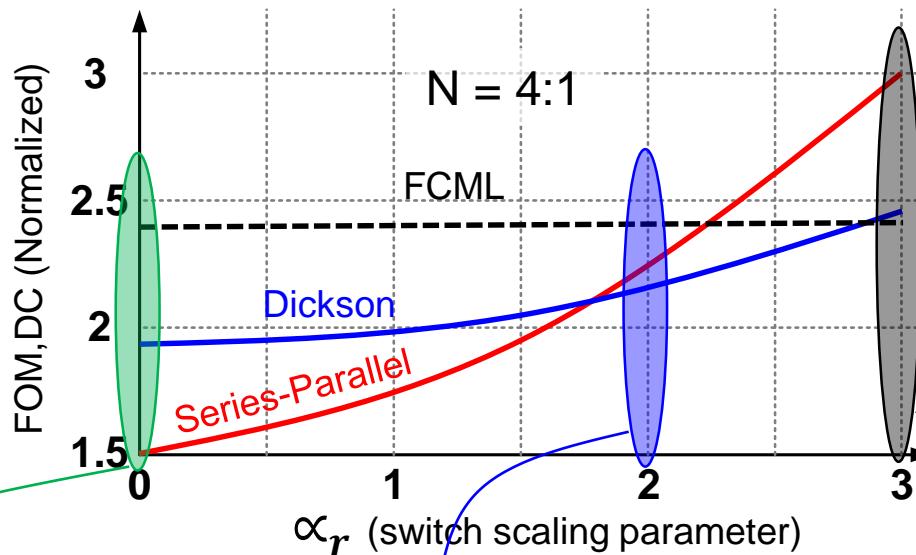
Dickson-Based Better →



$\alpha_r = 3$
(Constant field scaling)

Topology Comparison (Fixed Passive Volume)

Versus α_r @ N = 4:1 Step Down VCR



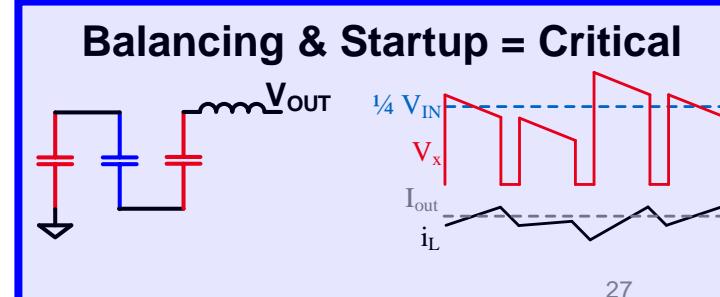
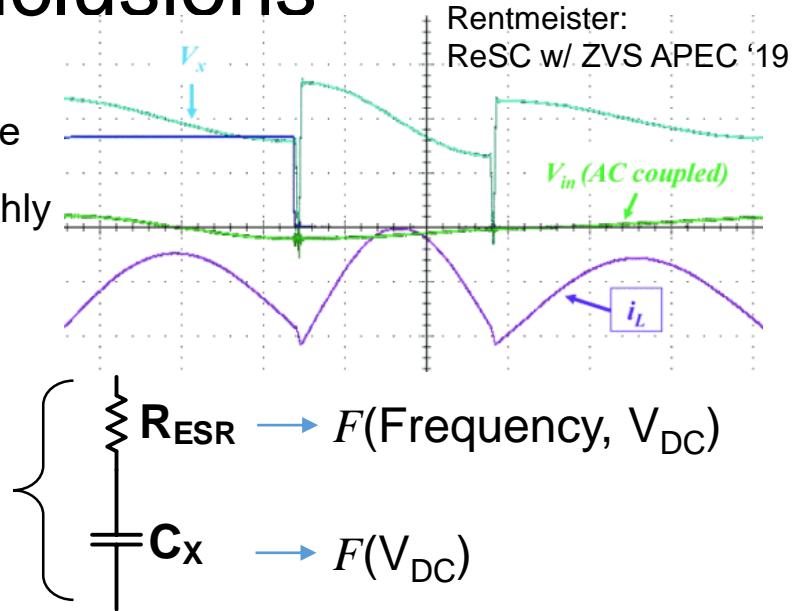
- @ $\alpha_r = 0$, All same switches
 - **Series Parallel** = Best: no penalty for HV switches

- @ $\alpha_r = 2$, Cascode scaling:
 - **Dickson** ~ Better: use of switches more effective

- @Long-channel (constant field):
 - **FCML** starts to win (all same *low* voltage switches)

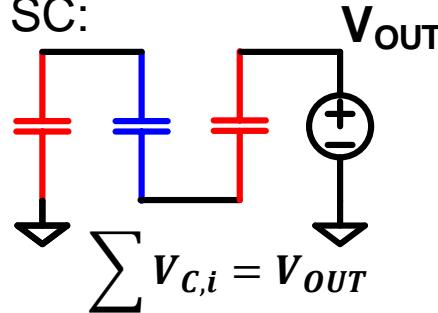
Caveats to Analysis/Conclusions

- There may be further constraints beyond power loss...
e.g. if 'switch sizes' are dominant... or more generally, the higher weighting on 'active utilization ... push toward Dickson/ladder, CW; if passive size is critical or more highly weighted, push towards series parallel
- Bottom plate (CV^2 , C_{oss}) losses \rightarrow important factor!
 - ZVS in hybrid topologies:
[Blackwell et al., COMPEL '18]
[Rentmeister et al., APEC '19]
- Resistive losses in capacitors \rightarrow non-negligible!
[Coday et al., COMPEL '18; APEC '20]
- Variety of other challenges limit implementation(s)
 - Gate driving complexity [Wicht, Pilawa, HP Le, Stauth, others]
 - Flying capacitor voltage balance [Meynard, Prodic, Corradini, Ruderman, Reusch, Stillwell, Pilawa, others]
 - Startup/precharge [Prodic, Stauth, Schaef, Pilawa]
 - Assembly: complexity and interconnect losses



Dynamics and Voltage Balance

SC:



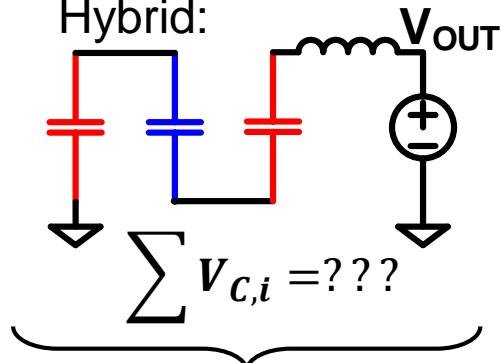
@ Pure SC

- Rigid voltage loops force unique voltages
- Balanced with 0th to 1st order dynamics

@ Hybrid SC

- Inductor decouples C_{fly} Voltages
- Possible imbalance
- Can have 'high-order' dynamics (poles)

Hybrid:

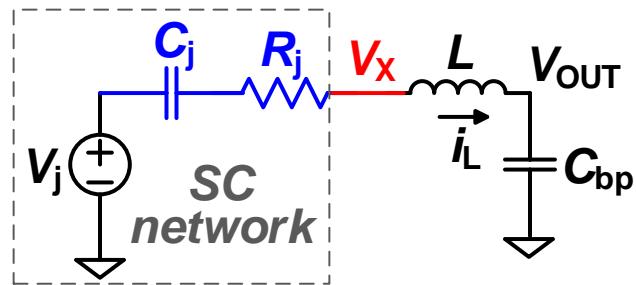


Inductor decouples 'rigid' voltage constraints

→ 'N-level' FCML converter: 'N' independent energy storage elements (poles, eigenvalues)

→ Compare to Buck which is generally 2nd order!

Dynamics and Voltage Balance



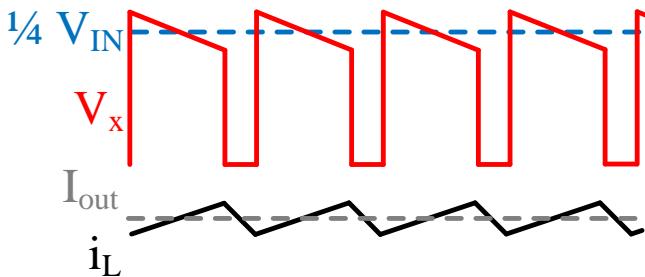
Weak negative feedback from system R_{ESR} :
→**Natural balance** (but this **is slow**)
→Not always reliable → Possibly need active FB

@ Minor operating asymmetries

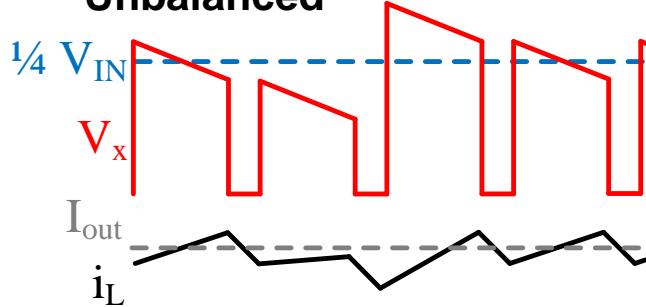
(duty cycle, rise time, source/load imped., transients)

- **Capacitor voltages drift** from nominal states
- **Higher current ripple** in inductor
- **Higher voltage stress** in SC network

Balanced



Unbalanced



Dynamics and Balancing

Large Body
of Past Work:

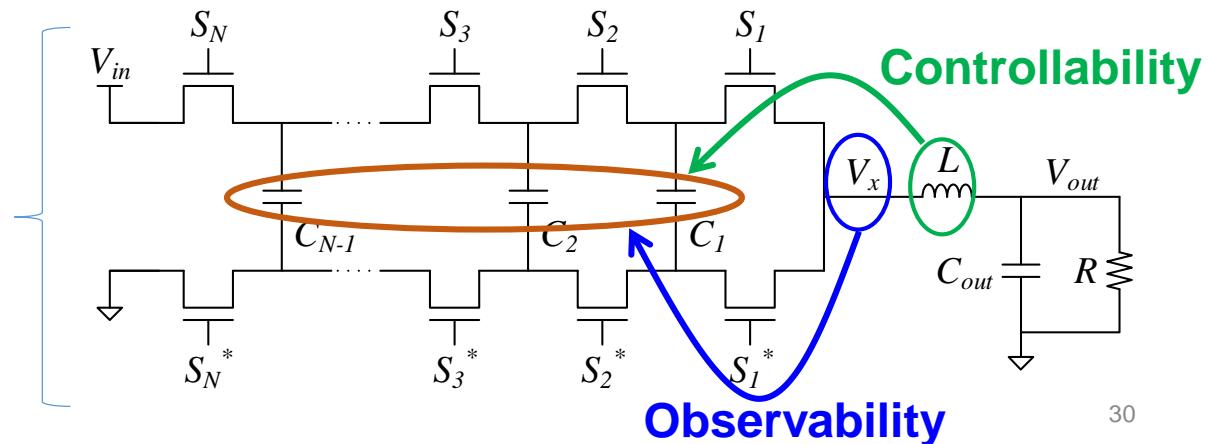
General Modelling + Natural Balance

- [Wilkinson & Meynard PESC '06]
- [Ruderman et al., ISIE '10]
- [Lei, Ye, Pilawa et al., TPEL '18, '22]
- [Das, H.P. Le, Maksimovic et al., '19]
- [Salinas, TIE '16]
- Many others...

Updated Perspective
(modern control)
[Xia & Stauth, APEC '19,
COMPEL '19]

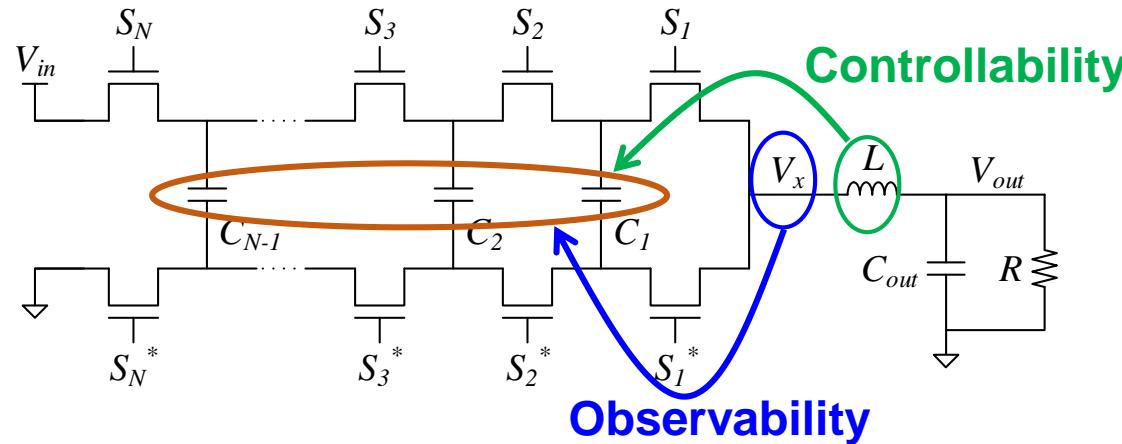
Current & Voltage Mode Techniques

- [Meynard TIE '02]
- [Kesarwani & Stauth COMPEL '15]
- [Reusch ECCE '09]
- [Rentmeister & Stauth APEC '17]
- [Stillwell & Pilawa, TPEL '19]
- [Lu, Prodic et al., COMPEL '19]
- [others...]



Modern Control Metrics:

[Xia et al., “State Space Analysis of Flying Capacitor Multilevel DC-DC Converters for Capacitor Voltage Estimation,” APEC ’19]

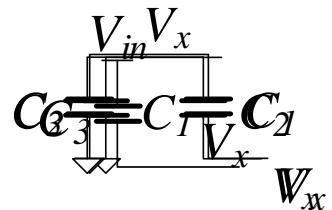
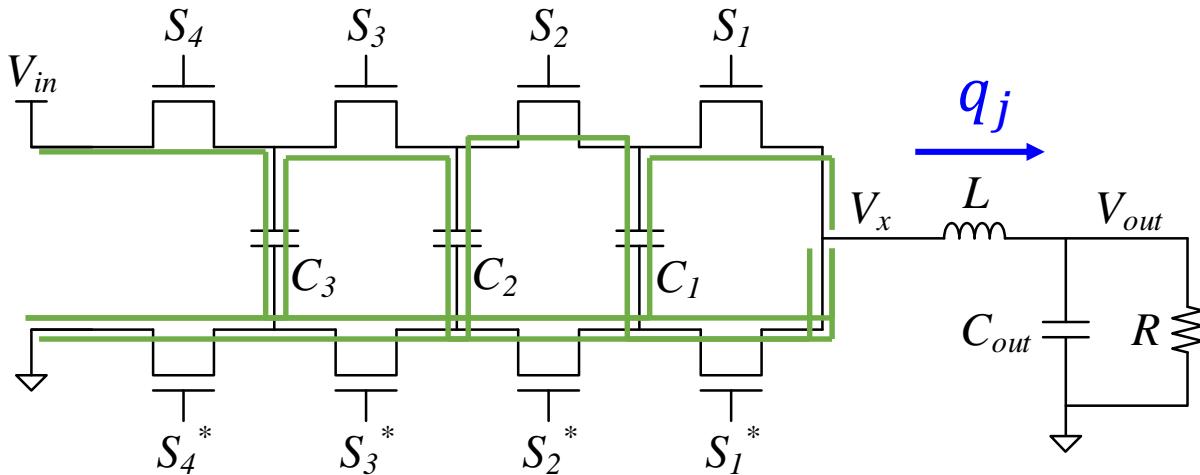
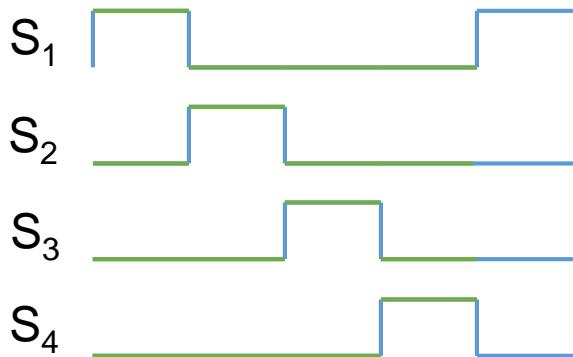


Observability: measurements of V_x are sufficient to determine ‘average’ capacitor voltage states (and input voltage V_{in})

Controllability: some current (or charge) ‘trajectory’ (phase durations, inductor current etc) is ‘capable’ of regulating ‘average’ capacitor voltage states

Example: 5-Level FCML

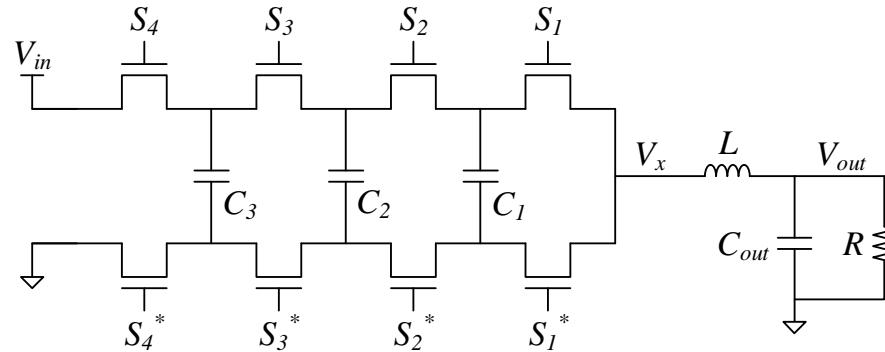
$$D = \frac{1}{4}$$



Phase 4

$$V_x = V_{C3} - W_{C2}$$

Example: 5-Level FCML



$$\begin{bmatrix} V_{C_1}[k+1] \\ V_{C_2}[k+1] \\ V_{C_3}[k+1] \end{bmatrix} = \begin{bmatrix} V_{C_1}[k] \\ V_{C_2}[k] \\ V_{C_3}[k] \end{bmatrix} + \underbrace{\begin{bmatrix} -\frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 \\ 0 & -\frac{1}{C_2} & \frac{1}{C_2} & 0 \\ 0 & 0 & -\frac{1}{C_3} & \frac{1}{C_3} \end{bmatrix}}_{\left. \right\{ q_1[k] \\ q_2[k] \\ q_3[k] \\ q_4[k] \right\}} \quad \left. \right\{ q_1[k] \\ q_2[k] \\ q_3[k] \\ q_4[k] \right\}$$

*q and C values
do not affect
controllability*

Observability & **Controllability** both dictated by the rank of this matrix
(more details in the paper)

Full State Space Formulation

$$V_C(k+1) = A \cdot V_C(k) + B \cdot q(k)$$
$$V_x(k) = C \cdot V_C(k) + D \cdot q(k) + W \cdot V_{in}$$

Observability \leftrightarrow **Controllability**

(Capacitor voltage estimation) (Active/natural balance)

$$\mathcal{O} = [C \quad CA \quad \dots \quad CA^{n-1}]^T$$

Depends on rank(C)

$$\mathcal{C} = [B \quad AB \quad \dots \quad A^{n-1}B]$$

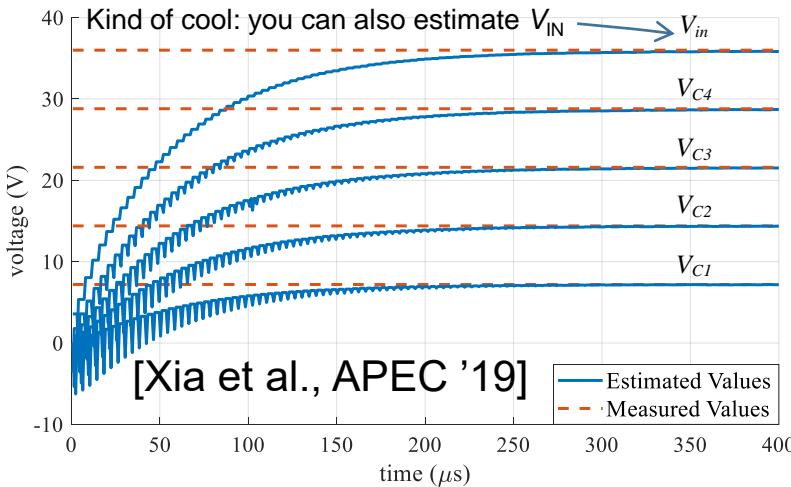
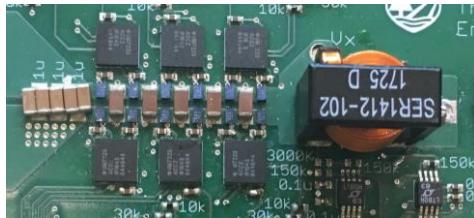
Depends on rank(B)

Takeaways

- **Observability** and **Controllability** have **same underlying criterion**
- Same conclusion as prior (more complicated) literature
- Can leverage to study dynamics and implement feedback

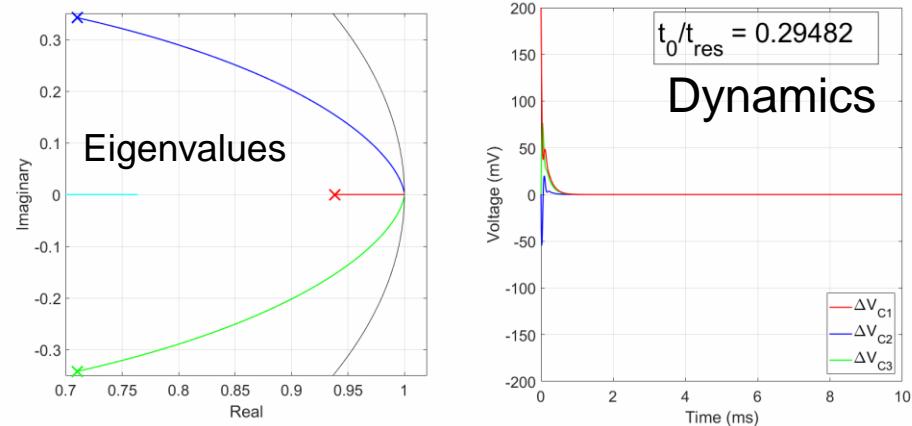
Opportunities Leveraging Control Metrics

Observability: determine C_{fly}
voltage + V_{IN} from samples of V_X



Note: above estimation appears slow, but we have underlying IIR filter running; with diff't filter BW, in principle these estimates can be quite fast!

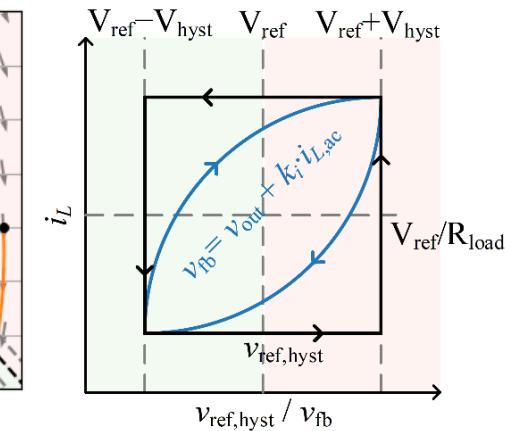
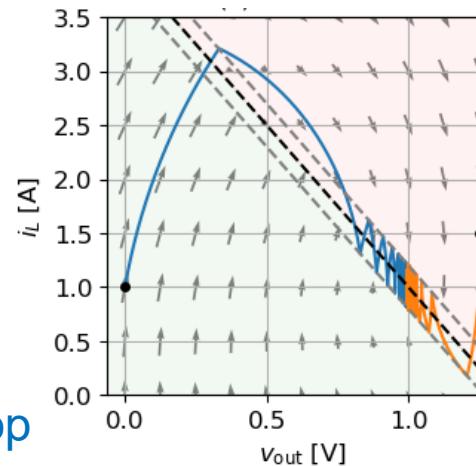
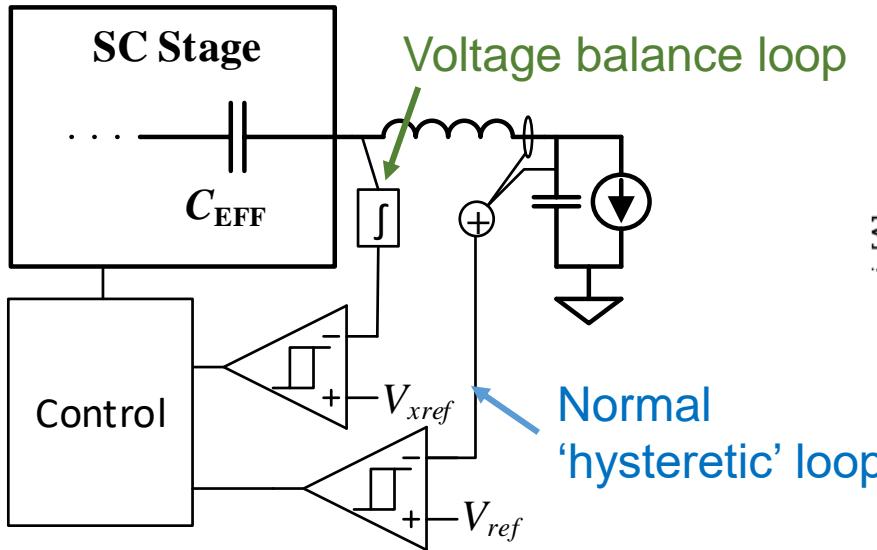
Controllability + Natural Balance:
[Xia et al., COMPEL '19]



- Methods allow to determine system dynamics → implement control schemes
- Methods show: whether control is feasible; point to addressing issues:
→ Modified PSPWM: fix certain topologies

Next Level → Nonlinear Control Extreme Fast Balancing + Regulation + Startup

- **Modified Ripple Injection:** like ‘sliding mode’ or ‘hysteretic’ control for buck converter...
...but add **feedback for flying cap voltage balance**

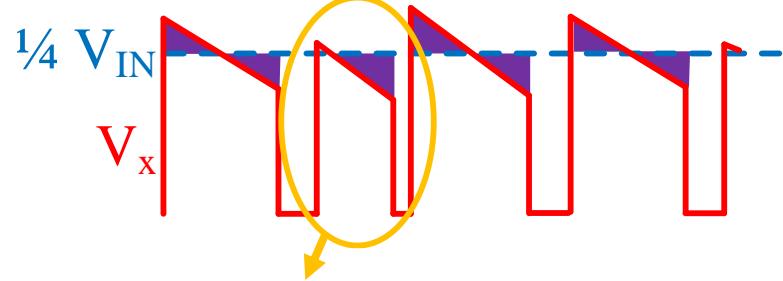
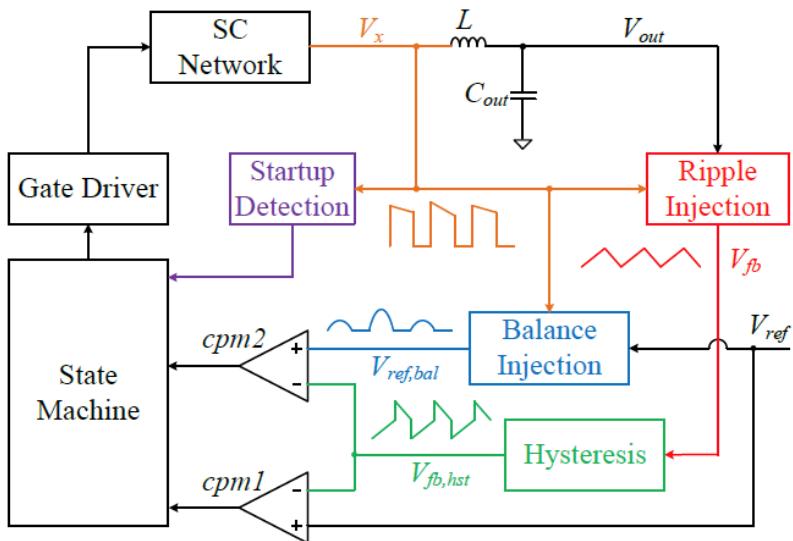


[Rentmeister CICC '20], [Xia ISSCC '21]

Nonlinear Control: Modified Ripple Injection

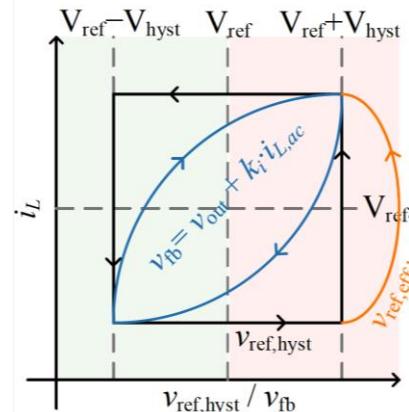
[Rentmeister CICC '20], [Xia ISSCC '21]

- **Hysteretic loop:** fast output transient resp.
- **Balancing loop:** fast reg. of cap voltages
- **Startup detection:** precharge caps (fast) to right voltages; prevent overvoltage stress

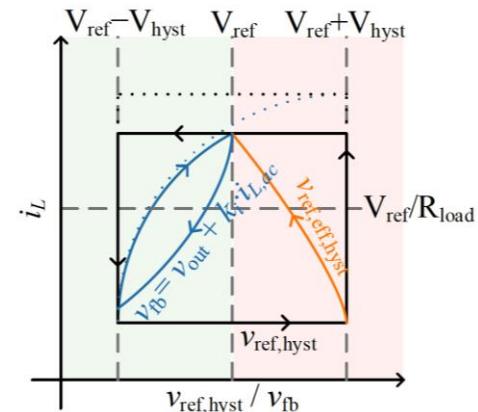


Integrate the switching node
→ inject back into the feedback controller.

Balanced



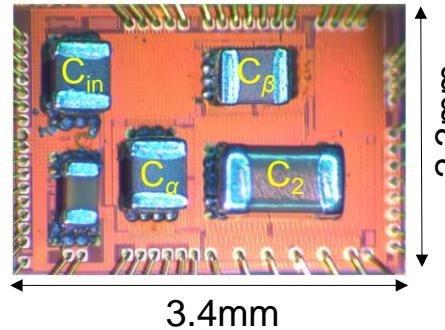
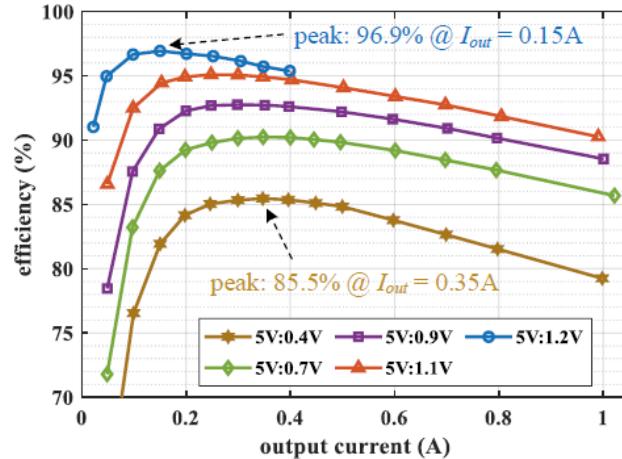
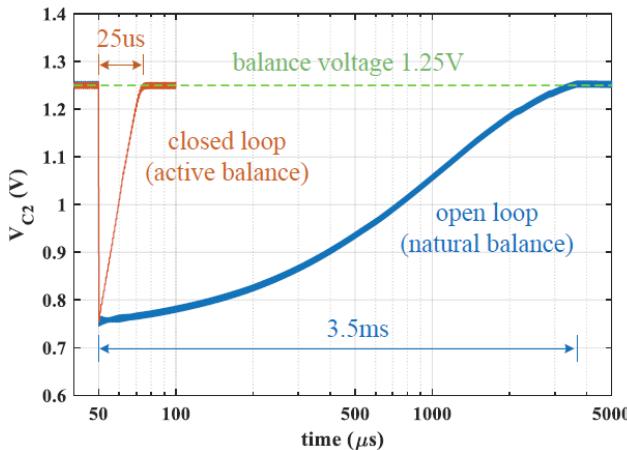
Imbalanced



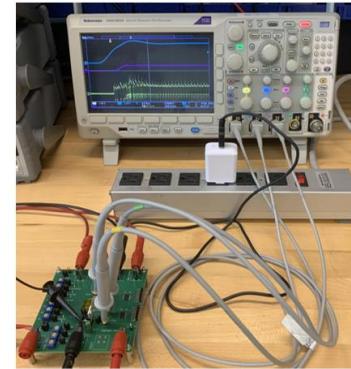
Results

Z. Xia and J. Stauth, “[17.1 A Two-Stage Cascaded Hybrid Switched-Capacitor DC-DC Converter with 96.9% Peak Efficiency Tolerating 0.6V/ \$\mu\$ s Input Slew Rate During Startup](#),” in 2021 IEEE International Solid-State Circuits Conference (ISSCC), 2021, pp. 256–258.

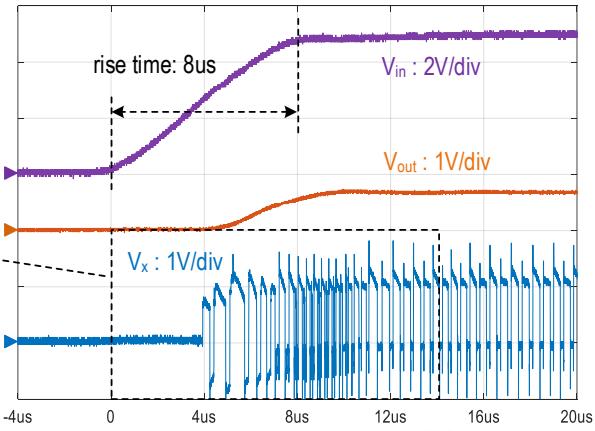
- Fast balancing dynamics ($>100x$ than nat. bal)
- Peak 96.9% efficiency
- $>85\%$ @ VCR = 5V:0.4V



Hard plug to USB cable:



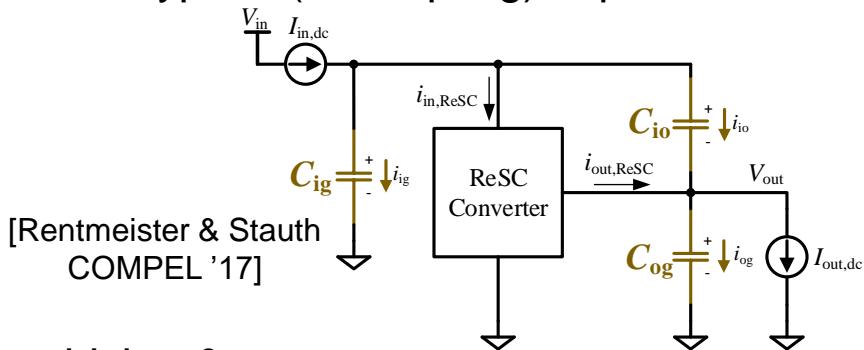
- Safe startup in $< 10\mu$ s
- startup ($V_{in}: 0V \rightarrow 5V$, $V_{ref} = 0.7V$, $I_{out} = 500mA$)



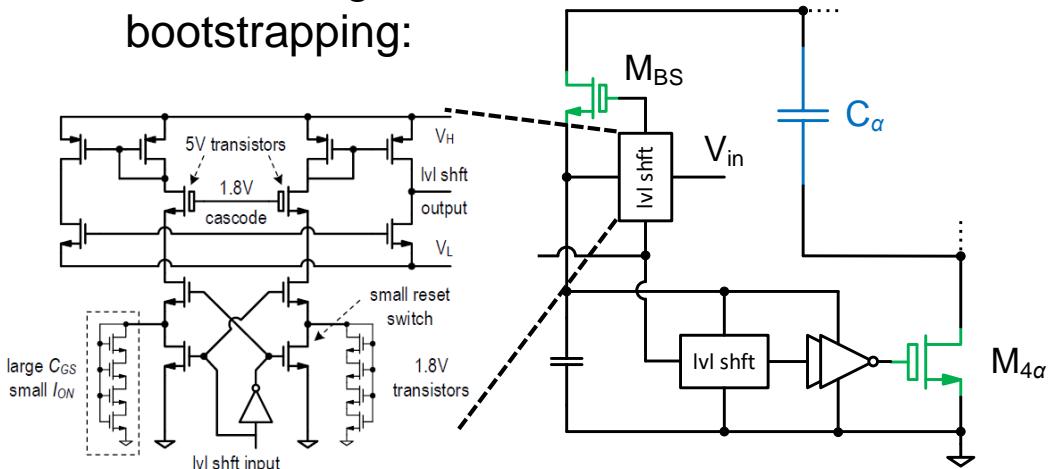
Challenges and Future Exploration

- Complicated circuits and switching networks
 - Better gate-drive, level shift, timing and control
 - Considerations of parasitics, layout, passive component integration (flying and bypass caps)
- Flying capacitor voltage balance
 - Huge challenges in normal operation
 - Worst in transient conditions: line, load
- How to startup without overstressing switches/passives
- Fast line/load transient response
 - Nonlinear control
 - Voltage balance feedback
 - Real-time balancing

Bypass (decoupling) capacitance



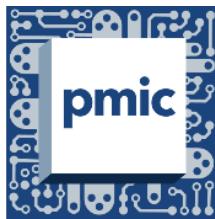
Gate driving &
bootstrapping:



Thanks!

Students who contributed to this work:

Prescott McLaughlin (current), **Ziyu Xia** (current), **Jan Rentmeister** (Google),
Hassan Kiani (Apple), **Sarah Pasternak** (ADI), **Kapil Kesarwani** (Eta Wireless),
Chris Schaef (Intel),



Power Management
Integration Center



THAYER SCHOOL OF
ENGINEERING
AT DARTMOUTH

UC San Diego
JACOBS SCHOOL OF ENGINEERING



Some References Related to this Talk

- J. T. Stauth, “[Pathways to mm-scale DC-DC converters: Trends, opportunities, and limitations](#),” in 2018 IEEE Custom Integrated Circuits Conference (CICC), 2018, pp. 1–8.
- S. R. Pasternak, M. H. Kiani, J. S. Rentmeister, and J. T. Stauth, “[Modeling and Performance Limits of Switched-Capacitor DC-DC Converters Capable of Resonant Operation With a Single Inductor](#),” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 4, pp. 1746–1760, Dec. 2017.
- P. H. McLaughlin, J. S. Rentmeister, M. H. Kiani, and J. T. Stauth, “[Analysis and Comparison of Hybrid-Resonant Switched-Capacitor DC-DC Converters With Passive Component Size Constraints](#),” *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3111–3125, Mar. 2021.
- Z. Xia and J. Stauth, “[17.1 A Two-Stage Cascaded Hybrid Switched-Capacitor DC-DC Converter with 96.9% Peak Efficiency Tolerating 0.6V/μs Input Slew Rate During Startup](#),” in 2021 IEEE International Solid State Circuits Conference (ISSCC), 2021, pp. 256–258.
- Z. Xia, et al., “[State Space Analysis of Flying Capacitor Multilevel DC-DC Converters for Capacitor Voltage Estimation](#),” 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 50-57, doi: 10.1109/APEC.2019.8722230.
- Z. Xia et al., “[Natural Balancing of Flying Capacitor Multilevel Converters at Nominal Conversion Ratios](#),” 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 2019, pp. 1-8, doi: 10.1109/COMPEL.2019.8769724.
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- M. H. Kiani and J. T. Stauth, “[Passive Component Modeling and Optimal Size Allocation for Hybrid-Resonant Switched Capacitor DC-DC Converters](#),” in 2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), 2018, pp. 1–8.
- M. H. Kiani and J. T. Stauth, “[Optimization and comparison of hybrid-resonant switched capacitor DC-DC converter topologies](#),” in 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), 2017, pp. 1–8.
- J. S. Rentmeister and J. T. Stauth, “[Bypass capacitance and voltage ripple considerations for resonant switched capacitor converters](#),” in 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), 2017, pp. 1–8.